DISAGGREGATED AND COMPOSABLE SOLUTIONS FOR DATA CENTERS

Gain insights into disaggregated and composable solutions with CDFP PCIe Gen 6 Interconnects for data centers.

Disaggregated And Composable Solutions For Data Centers

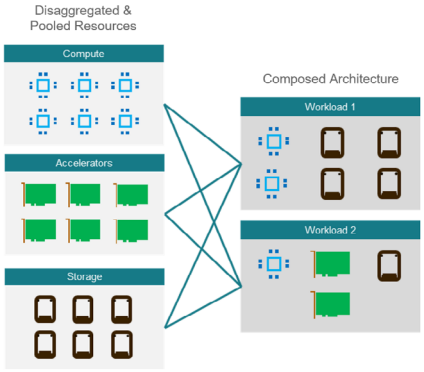
With the emergence and rise of big data, autonomous vehicles, industrial internet of things (IIoT) and generative AI (artificial intelligence) technologies, the demands for data computing, storage and network traffic continue to grow significantly. These demands drive global investment in data center infrastructure, with needs growing exponentially to sustain global data demands. Given increasing demand, data centers are carrying a significant amount of the workload, stressing existing infrastructures and accelerating the need for upgrades.

THE KEY CHALLENGES FACING DATA CENTERS

- Limited resources from data centers, like power, water and physical space
- Workload increases due to a large amount of operating end applications
- Cost and performance optimization

DISAGGREGATED AND COMPOSABLE ARCHITECTURES

Disaggregated and composable architectures leverage pooled resources of compute, memory, storage, and hardware acceleration. PCIe or CXL (Compute Express Link) switches connect the pooled resources into a large cluster and the resources can be configured in real time to match the needs of specific workloads. This results in cost and performance improvement by helping to eliminate stranded resources and allowing an increased buffer for demanding workloads. In traditional architectures once a CPU runs out of local memory, the workload needs to take advantage another CPU to access its local memory. In a disaggregated and composed architectures, the CPU can access its local memory and the pooled memory without the need of another CPU.



TARGET APPLICATIONS

- Pooled memory – JBOM (Just-a-Bunch-of-Memory)
- Clustering GPUs and AI accelerators and connecting to them to CPU head nodes– JBOG (Just-a-Bunch-of-GPUs)
- Storage arrays – JBOD (Just-a-Bunch-of-Disks) and JBOF (Just-a-Bunch-of-Flash)
- CXL switching and fabrics
- Disaggregated Network Interface Cards (NICs) – JBON (Just-a-Bunch-of-NICs)

BENEFITS OF CDFP TECHNOLOGY

Standard and multi-source form factor recognized by multiple organizations:

- Selected as external PCIe cabling form factor for PCIe Gen 5 and 6 by PCI-SIG (Peripheral Component Interconnect Special Interest Group)
- Defined in SNIA (Storage Networking Industry Association) under SFF-TA-1032 specification
- Form factor adopted in robust ecosystem by hyperscale cloud providers and OEMs

Specifically tuned for PCIe:

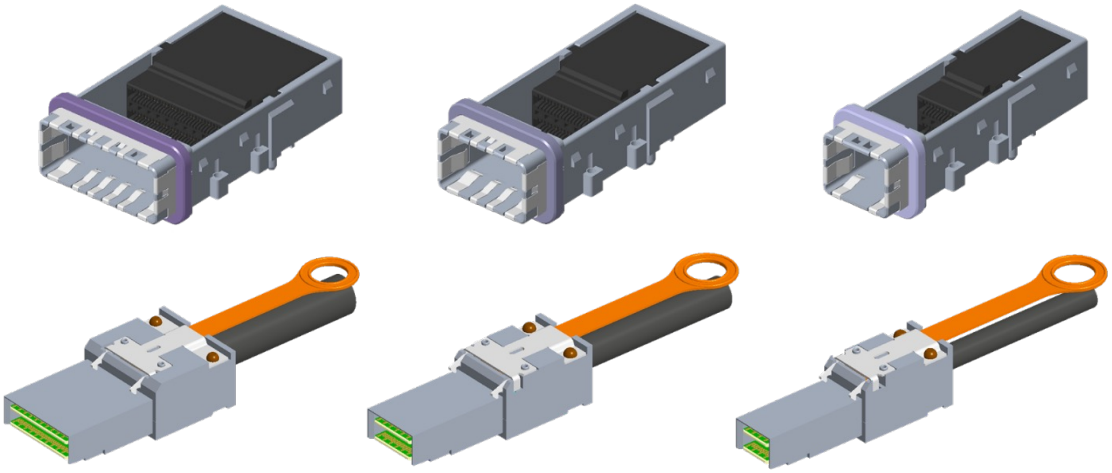
- Form factors supporting x16, x8, and x4 high speed lane counts
- 85Ω nominal impedance
- Offers the necessary sideband signals

Disaggregated And Composable Solutions For Data Centers

Wide ranging portfolio supporting application flexibility:

- Supports PCIe gen 4, 5 and 6
- Supports passive copper, active copper, and optical cabling solutions
- Allows for press fit (PCIe Gen 5) and SMT (PCIe Gen 6) PCB connectors
- Panel mount CDFP cable receptacle to enable over-the-board internal cabled connections
- Fits onto standard device form factors (PCIe Add-In-Card, OCP NIC TSFF, SFF-TA-1034, etc.)
- Flexibility in cable AWG to optimize signal integrity channel performance and mechanical cable routing

CDFP CONNECTOR & CABLE CONFIGURATIONS FOR PCIe GEN 5 & PCIe GEN 6



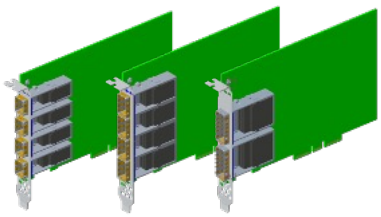
X16 – 120 POSITIONS | X8 – 68 POSITIONS | X4 – 44 POSITIONS

FORM FACTOR & DEVICE COMPATIBILITY

- CDFP is among the highest density interconnects for a x16 PCIe external cable currently on the market
- It is the only x16 form factor that fits within a PCIe AIC and OCP NIC
- It has the shallow depth of both x8 and x16 I/O connectors to best fit in OCP NiC 3.0 and half length PCIe AIC as well as allows for efficient routing from connector to PCIe AIC card edge
- Designed to support from x16 down to x1*

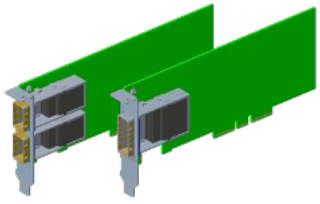
1x and x2 interface use the x4 connector

Full Height PCIe Card Electromechanical (CEM) AICs



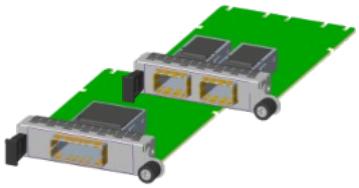
4 CDFP X4 (SINGLE) | 4 CDFP X8 (GANGED) | 2 CDFP X16 (SINGLE)

Low Profile PCIe CEM AICs



2 CDFP X8 (SINGLE) | 1 CDFP X16 (SINGLE)

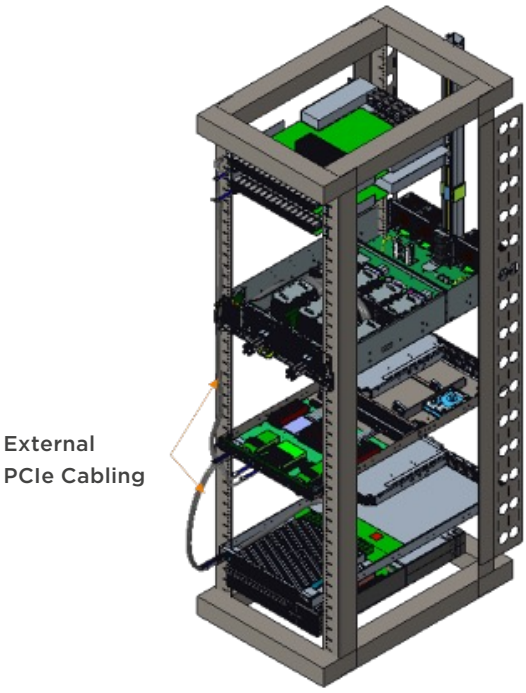
OCP NIC 3.0 TSFF



1 CDFP X16 (SINGLE) | 2 CDFP X8 (SINGLE)

FUTURE OF CDFP & EXTERNAL PCIe TECHNOLOGIES

Today, CDFP technology enables a x16 link width within a single port and will be scalable to support x8 and x4 channels. As the industry upgrades from PCIe Gen 5 to PCIe Gen 6, the connector footprint migrates from press-fit to surface mount technology (SMT). The passive copper cable is typically used for current hyperscale/cloud applications, but next generation data center architectures are driving longer physical reaches. These longer lengths are enabled by active copper and optical cabling.
A panel mount cable receptacle enables OTB (over-the board) internal cabling options. This is typically cabled near the CPU, PCIe retimer, or CXL switch. Market discussions around PCIe Gen 7 are ongoing and TE Connectivity (TE) is actively developing CDFP Gen 7 capability.



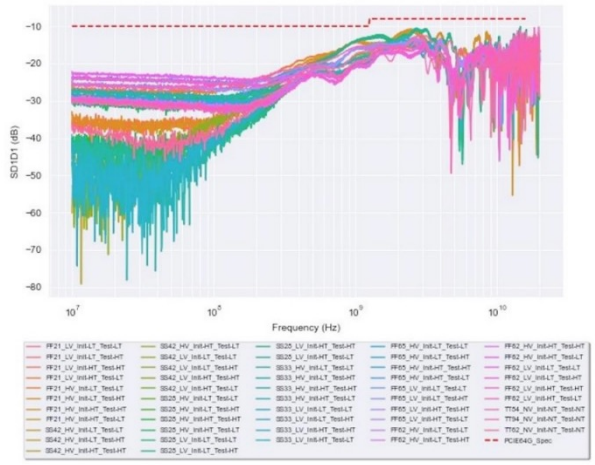
MARVELL PCIE GEN 6 RETIMER TEST CHIP

- 8-lane PCI-Express Gen-6 and CXL protocol-aware low-latency retimer
- Compatible with PCIe Gen 6/5/4/3/2/1
- Supports 64/32/16/8/5/2.5 Gigatransfers per second (GT/s) data rates
- Flexible link bifurcation including 1x8, 2x4, 4x2
- High performance exceeds PCIe specification requirements:
  - Extend reach by >32dB at 64 GT/s
  - Fully programmable TX (transmit) FIR (finite impulse response)
  - Equalization by CTLE (continuous time linear equalization) & Real-Time DFE (decision feedback equalizer) Adaptation

CHIP PERFORMANCE

- Setup: EVB1 – MXP – Channel – MXP – EVB2
- Note: Performance as measured – Not optimized. Further tuning ongoing

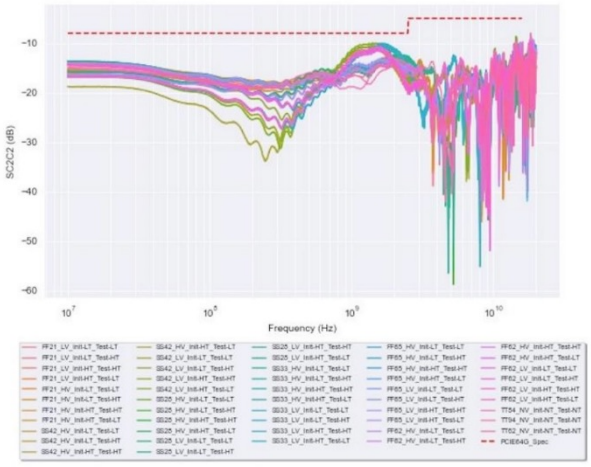
Channel	IL@64G	BER_max @PCIe_64G	BER_max @PCIe_32G
ISI BT31”	33.41db	2.44E-08	<1.0E-14
ISI BT17” + 6.5”	27.67db	5.70E-09	<1.0E-14
ISI BT12” + 8db (4db + 2db + 2db short boards)	33.19db	1.45E-08	<1.0E-14
ISI BT9” + 4db short board	17.79db	2.07E-10	<1.0E-14
Short Trace	3.29db	1.74E-11	<1.0E-14



PCIe 64GT/S TX DIFFERENTIAL MODE RETURN LOSS

PCIe 64GT/S TX COMMON MODE RETURN LOSS

PCIe 64GT/S RX DIFFERENTIAL MODE RETURN LOSS



PCIe 64GT/S RX COMMON MODE RETURN LOSS

PCIe 6 TEST CHIP EVB

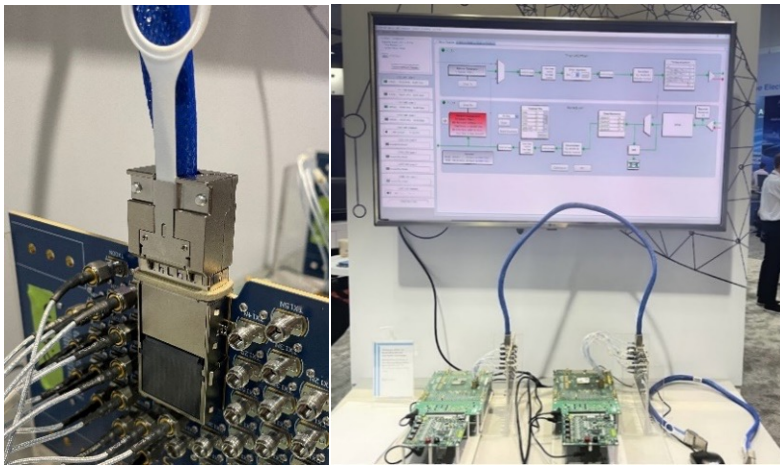
- x4 PCIe 6 SerDes IP
- PC-based GUI (graphical user interface) to control and monitor
- Ability to generate and check PRBS (pseudo-random binary sequence)
- Eye scan capability

TE'S CABLED PCIe 6 DEMO AT DESIGNCON 2023

PCIe Gen 6 Running over 1m Gen 5 CDFP Cable

- Silicon used: Marvell PCIe 6.0 SerDes (64GT/s PAM4)
- Cable: 30AWG 1m long (longer lengths achievable)
- BER 4.7x10-13 (running for ~3 hours)

Demo scheduled at OCP Global Summit 2023 using TE Connectivity 4m Gen 5 CDFP cable running at 64GT/s (PCIe Gen 6) driven by Marvell's PCIe Gen 6 SerDes



WHY TE FOR CDFP SOLUTIONS

TE's high speed I/O portfolios offer a variety of early-to-market and end-to-end solutions that allow users to meet key demands in performance, density, resource capacity, expandability, and cost. With a global manufacturing footprint, TE can offer stable production and supply while retaining high quality and continuous improvement. From online to offline sales, TE can provide quick response and one-stop shop for customers via a broad sales, technical support and distribution network.

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