QSFP Timing Verification

2156043-1 Firmware Rev 13.3

Purpose

Verification of SFF-8436 Timing Requirements

Scope

I/O Timing for Soft Control and Status Functions on QSFP+ Transceiver Firmware Rev 13.3

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Change History

Issue	Date	Author	Description
A	11-1Oct-2011	J.Walz	Creation of document
B			
C			

References

Document No	Document Title
	SFF-8436

1 Abstract

QSFP MSA specifies 3 sets of timing requirements

- QSFP 2-Wire Timing Specification
- QSFP Memory Specification
- I/O Timing for Soft Control and Status Functions

The 2-wire interface timing is part of the I^2C implementation in the used μController.

The presented measurements verify the Soft Control and Status Functions timing.

2 Summary

QSFP MJDC Firmware Rev 13.3 meets all QSFP MSA timing requirements.

3 Test Configuration

The test uses a QSFP module on a TE Eval Board with the optical signal from the DUT passing an optical switch and looped back into the DUT.

The oscilloscope monitors

- Tx Signal
- Rx Signal
- Signal Generator Trigger
- ResetL
- IntL
- ModSelL

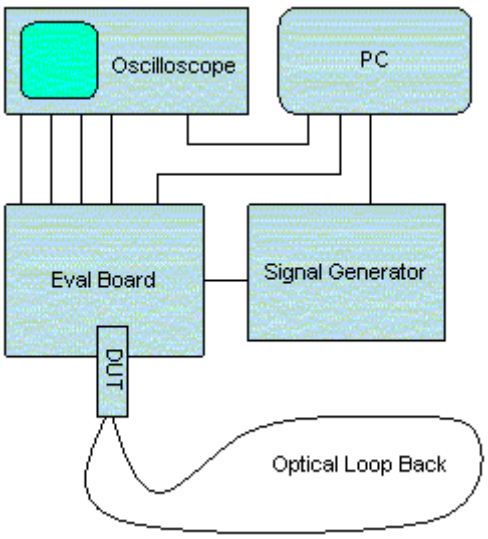


Fig 1 Timing Test Setup

The Test Application controls QSFP settings and triggers and monitors QSFP Status Interrupt Flags and Module and Channel Monitors.

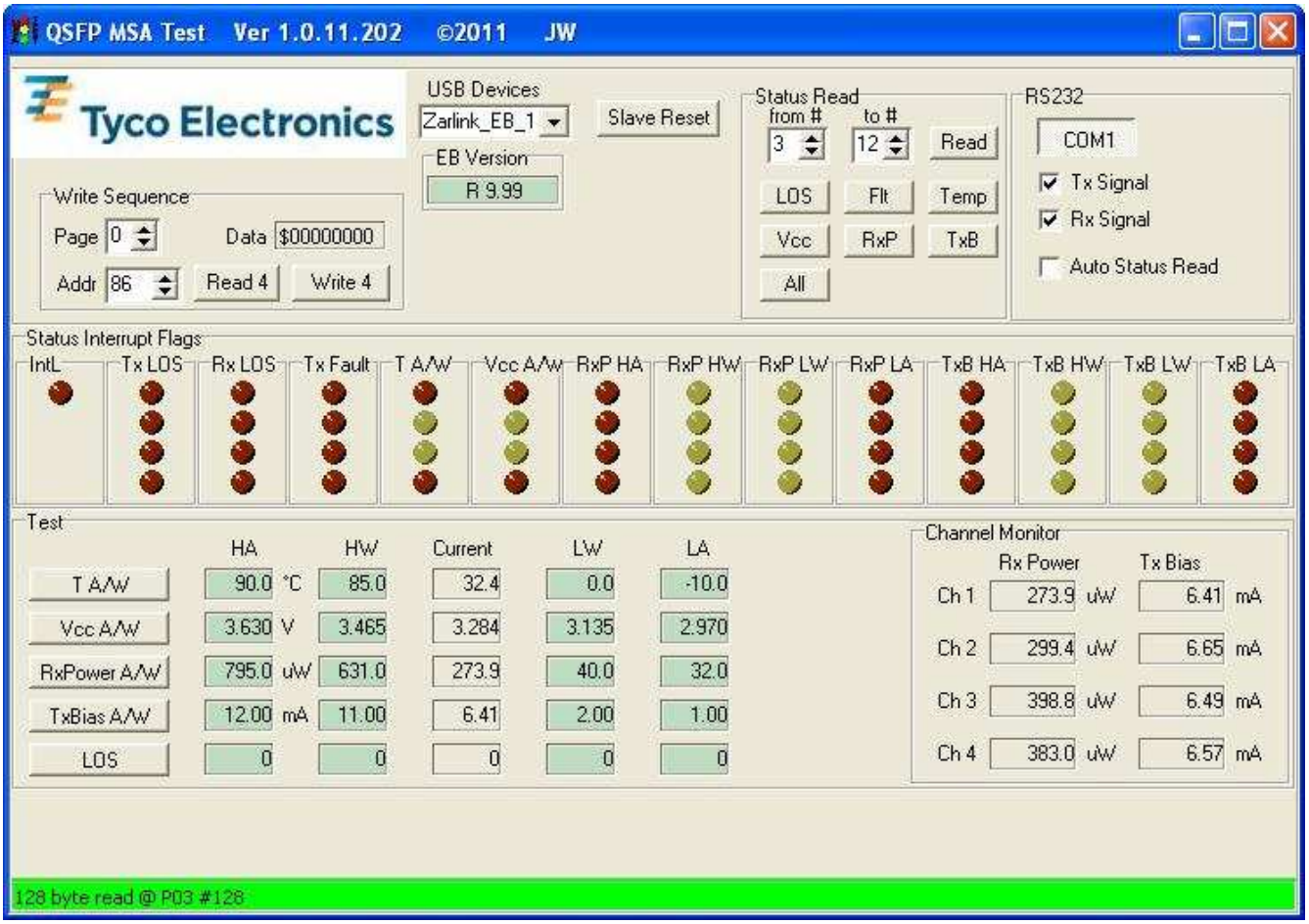


Fig 2 QSFP Timing Test Application GUI

4 SFF-8436 Timing Specification

4.1 QSFP 2-Wire Timing Specification

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	f_{SCL}	0	400	kHz	
Clock Pulse Width Low	t_{LOW}	1.3		us	
Clock Pulse Width High	t_{HIGH}	0.6		us	
Time bus free before new transmission can start	t_{BUF}	20		us	Between STOP and START
START Hold Time	$t_{HD,STA}$	0.6		us	
START Set-up Time	$t_{SU,STA}$	0.6		us	
Data In Hold Time	$t_{HD,DAT}$	0		us	
Data In Set-up Time	$t_{SU,DAT}$	0.1		us	
Input Rise Time (400kHz)	$t_{R,400}$		300	ns	From (VIL,MAX - 0.15) to (VIH,MIN + 0.15)
Input Fall Time (400kHz)	$t_{F,400}$		300	ns	From (VIH,MIN + 0.15) to (VIL,MAX - 0.15)
STOP Set-up Time	$t_{SU,STO}$	0.6		us	
ModSelL Setup Time	Host_select_setup	2		ms	Setup time on the select lines before start of a host initiated serial bus sequence
ModSelL Hold Time	Host_select_hold	10		us	Delay from completion of a serial bus sequence to changes of transceiver select status
Aborted sequence - bus release	Deselect_Abort	2		ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence),to the QSFP module releasing SCL and SDA

Table 1: QSFP 2-Wire Timing Specification

Parameter	Symbol	Min	Max	Unit	Conditions
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	us	Maximum time the QSFP module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	t_{WR}		40	ms	Complete (up to) 4 Byte Write
Endurance (Write Cycles)		50 k		cycles	70 °C

Table 2: QSFP Memory Specification

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on[2], hot plug or rising edge of Reset until the module is fully functional[3] This time does not apply to non-Power Level 0 modules in the Low Power State.
Reset Init Assert Time	t_reset_init	2	us	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[2] until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on[2] to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional[3]
LPMode Assert Time	ton_LPMode	100	us	Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption enters Power Level 1
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	us	Time from clear on read[4] operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set (value = 1b)[1] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared (value = 0b)[1] until associated IntlL operation resumes
Application or Rate Select Change Time	t_ratesel	100	ms	Time from change of state of Application or Rate Select bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set (value = 1b)[1] until module power consumption enters Power Level 1
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared (value = 0b)[1] until the module is fully functional[3]
Note 1. Measured from falling clock edge after stop bit of write transaction.				
Note 2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 6.				
Note 3. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted. The module should also meet optical and electrical specifications.				
Note 4. Measured from falling clock edge after stop bit of read transaction.				

Table 3: I/O Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	80	us	Time from loss of Rx input signal until the squelched output condition is reached. See clause 3.1.3.1.
Rx Squelch Deassert Time	toff_Rxsq	80	us	Time from resumption of Rx input signals until normal Rx output condition is reached. See clause 3.1.3.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached. See clause 3.1.3.2.
Tx Squelch Deassert Time	toff_Txsq	400	ms	Time from resumption of Tx input signals until normal Tx output condition is reached. See clause 3.1.3.2.
Tx Disable Assert Time	ton_txdis	100	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 1b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled.
Note 1. Measured from falling clock edge after stop bit of write transaction.				

Table 4: I/O Timing for Squelch and Disable

5 Verification Measurements

5.1 QSFP 2-Wire Timing Specification

5.1.1 Clock Frequency, Pulse Widths and Hold Times

For verification of I2C timing compliance, a Telos Tracii XL 2.0 and I2C Negative Tester has been used.

The test covers

- Multiple reads of various number of bytes
- Master Clock Diversifying with arbitrary 1 - 100 ms delay in clock pulses (asynchronous clocking)
- Master Timing 100 kHz – 400 kHz.
  Several combinations of $t_{HD;DAT}$, $t_{SU;DAT}$, and t_{HIGH} with min and max values conform to std and fast mode devices I2C-Bus Spec Ver 2.1, Jan 2000 and Rev 03, 19 June 2007
- Master Speed (bitrates 1000 – 400000 Hz)

All tests pass successfully.

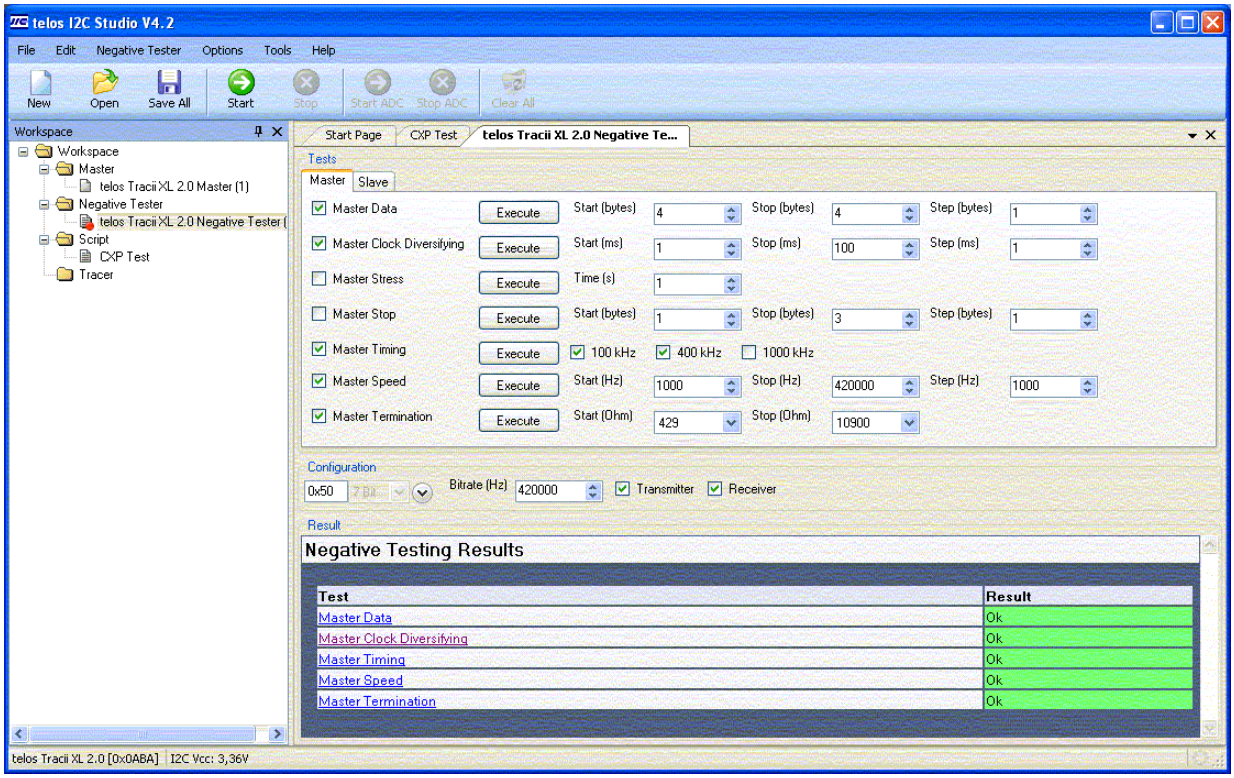
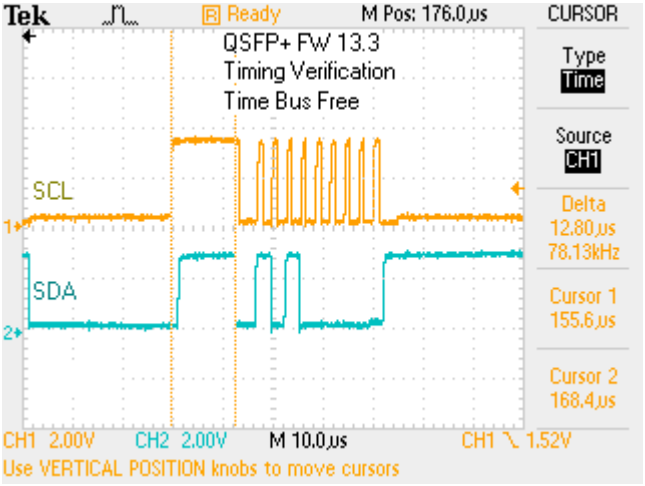


Fig 3 Telos I2C Negative Tester

5.1.2 Time Bus Free

This was tested with a configurable Bus Free Time, recording the shortest possible Bus Free Time with successful communication.



Parameter	MSA		Measurement	
Time Bus Free	≥ 20	µs	≥ 13	µs

Table 5: Time Bus Free

5.1.3 ModSelL

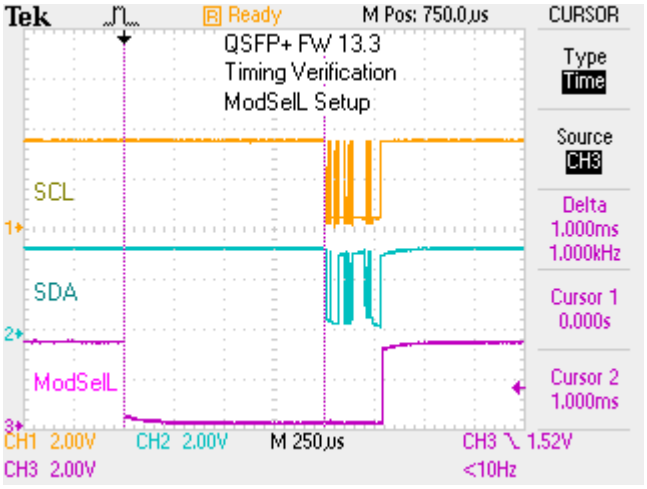


Fig 4 ModSelL Setup Time

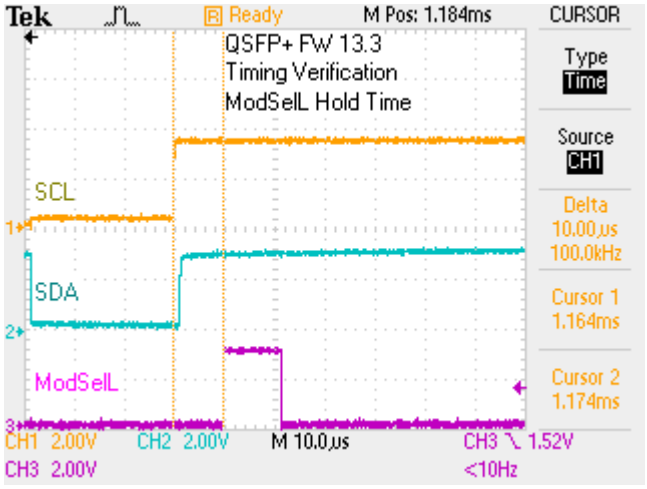


Fig 5 ModSelL Hold Time

Parameter	MSA		Measurement	
ModSelL Setup Time	≥ 2	ms	≥ 1	ms
ModSelL Hold Time	≥ 10	µs	≥ 10	µs

Table 6: ModSelL

The tests pass successfully with times shorter than required.

5.2 QSFP Memory Specification

5.2.1 Clock Stretching and Complete Write

Fig 6 - Fig 7 show 2 typical cases of clock stretching within a complete 4 byte write and read cycle

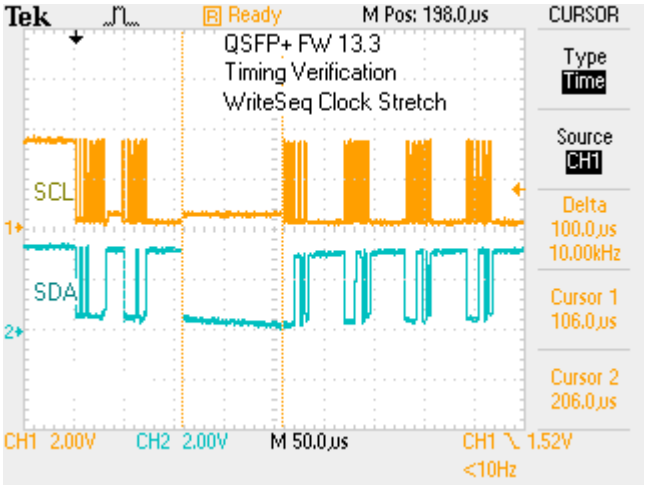


Fig 6 Write Sequence clock stretching

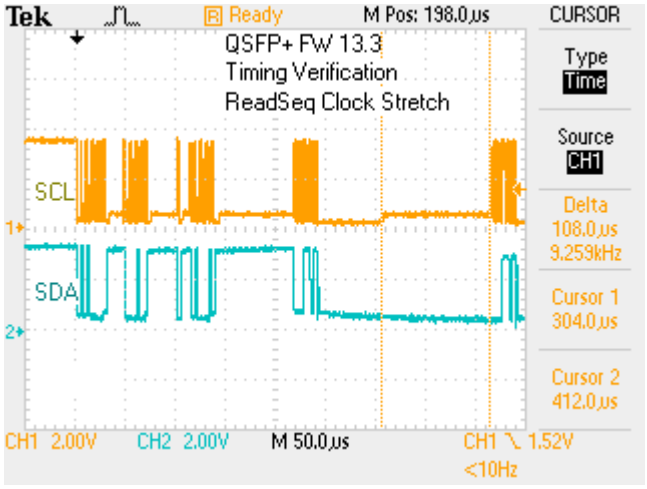


Fig 7 Read Sequence clock stretching

Parameter	MSA		Measurement	
Clock Stretching	≤ 500	µs	≤ 200	µs

Table 7: Clock Stretching

A complete write cycle of max 4 byte is done in less than 1 ms, as shown in Fig 8

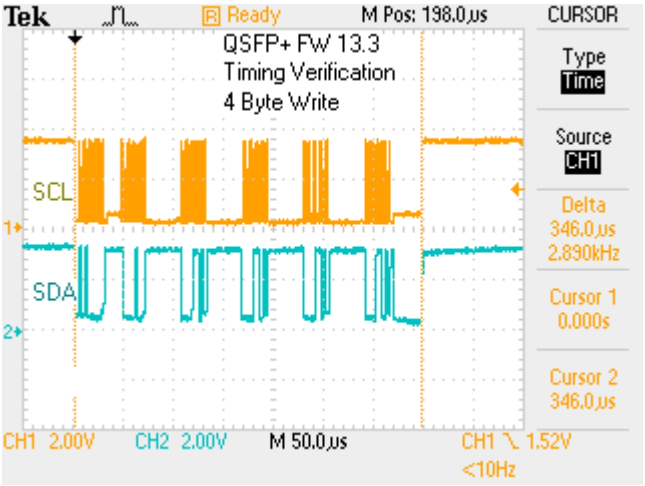


Fig 8 Complete 4 byte Write Cycle

Parameter	MSA		Measurement	
Complete 4 byte Write Cycle	≤ 40	ms	≤ 1	ms

Table 8: Write Cycle

5.3 I/O Timing for Soft Control and Status Functions

5.3.1 Initialization Time

Fig 9 shows the ResetL pulse of 2 µs. After approx 13 ms, I/O ports are initialized and IntL is asserted.

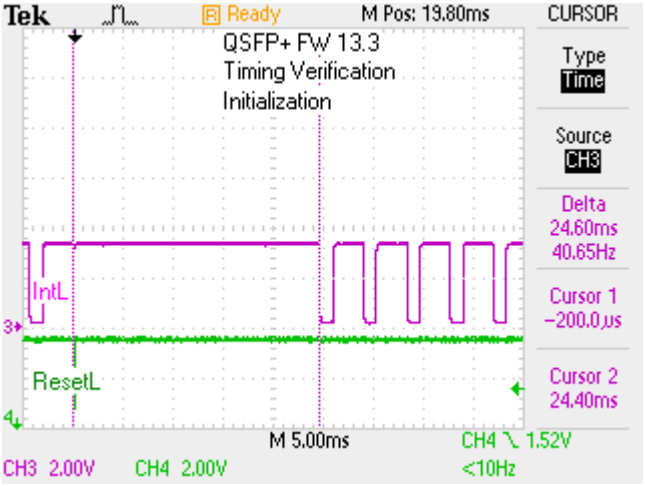


Fig 9 ResetL and initialization

An IntL test Pulse has been introduced to demonstrate initialization time and the main loop period

After approx 25 ms, IntL is released. At that time, initialization is done and the module is ready for communication. Main loop execution time is approx 3.5 ms

Parameter	MSA		Measurement	
Reset Init Assert Time	2	µs	2	µs
Initialization Time	≤ 2000	ms	< 1000	ms
Serial Bus Hardware Read Time	≤ 2000	ms	< 1000	ms
Monitor Data Read Time	≤ 2000	ms	< 1000	ms
Reset Assert Time	≤ 2000	ms	< 1000	ms

Table 9: Initialization time

5.3.2 IntL Assert Time

Fig 10 shows the Tx Electrical Signal being switched off, the corresponding Rx Out signal and the resulting IntL assertion. IntL reacts within a few ms.

For an error condition related to Temperature, Vcc, Rx Power or Tx Bias, the IntL assertion time is related to the main loop execution time, which is in the order of 3.5 ms.

Due the optical loop back configuration and the fact, that Tx Squelch is not implemented, the Rx does not really squelch for the current test configuration due to the remaining noise in the not squelching Tx signal. However, Rx reaction time is clearly shown in the Rx Out signal trace.

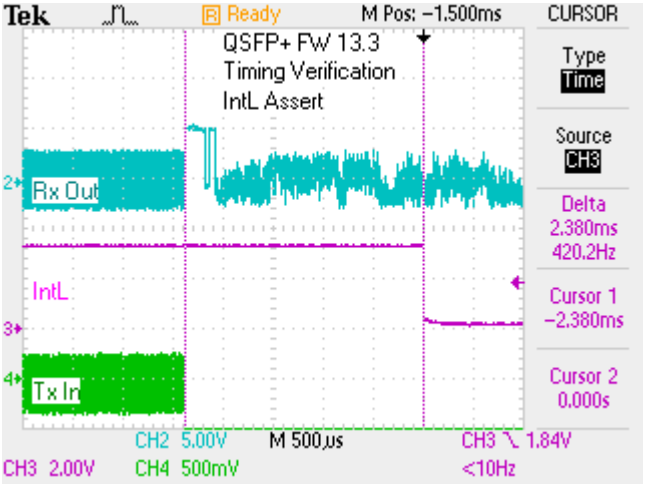


Fig 10 IntL Assert on Tx and Rx LOS

Parameter	MSA		Measurement	
IntL Assert Time on Tx Fault/LOS and Rx LOS	≤ 200	ms	< 4	ms
IntL Assert Time on T, Vcc, Rx Power, Tx Bias	≤ 200	ms	< 4	ms

Table 10: IntL Assert Time

5.3.3 IntL Deassert Time

When latched Status Interrupt Flags are cleared, an immediate check for existing error conditions is performed. This instant check is necessary to be able to deassert IntL within the required 500 µs.

If no more error conditions are present, IntL is deasserted.

This check causes also a clock stretching, which is within the allowed 500 µs

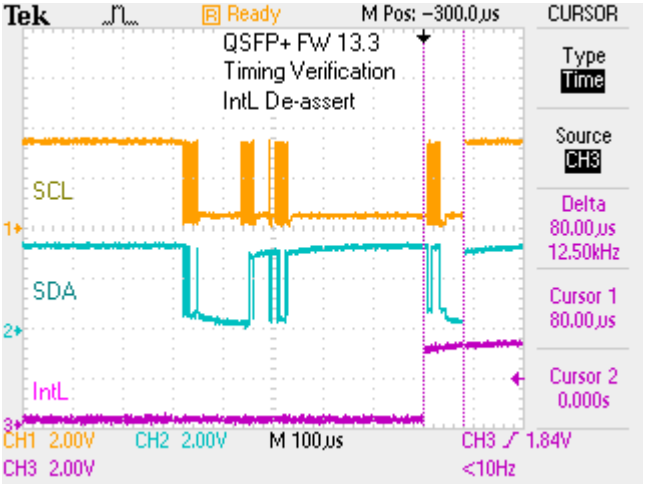


Fig 11 IntL Deaasert Time and Clock Stretching

Parameter	MSA		Measurement	
IntL Deassert Time on read operation	≤ 500	µs	< 100	µs

Table 11: IntL Deassert Time

5.3.4 Rx LOS Assert Time, Tx Fault Assert Time and Flag Assert Time

Due to the loop back configuration, the Rx optical signal input is linked to the Tx electrical signal input.

Thus, switching off Tx input signal causes an LOS for the Rx optical signal as shown in Fig 10. This is also true for a Tx Fault.

Setting Status Interrupt Flags is part of the tasks performed in the main loop. With a typical main loop execution time of 10 ms, setting a Status Interrupt Flag due to an error condition takes less than 4 ms.

Parameter	MSA		Measurement	
Rx LOS Assert Time	≤ 100	ms	< 4	ms
Tx Fault Assert Time	≤ 200	ms	< 4	ms
Flag Assert Time	≤ 200	ms	< 4	ms

Table 12: Rx LOS Assert Time, Tx Fault Assert Time and Flag Assert Time

5.3.5 Mask Assert Time

Processing memory changes when changed from host is also a task performed in the main loop and thus, executed approx every 3.5 ms. In worst case, the resulting IntL state change is processed in the following main loop, thus, within < 8 ms.

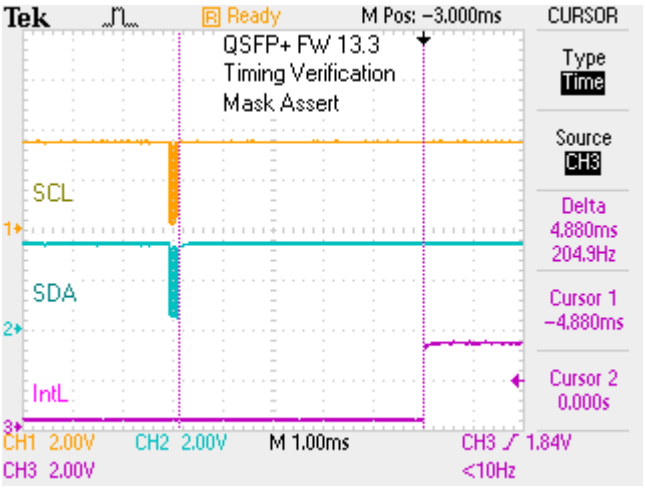


Fig 12 Rx LOS Mask Assert Time

Parameter	MSA		Measurement	
Mask Assert Time	≤ 100	ms	< 8	ms

Table 13: Mask Assert Time

5.3.6 Mask Deassert Time

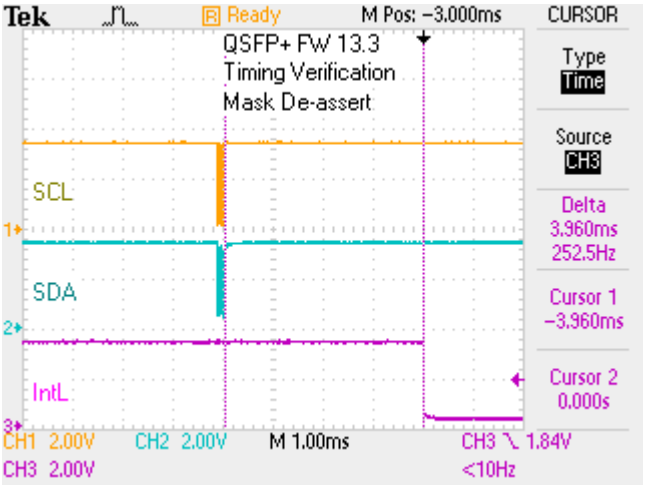


Fig 13 Mask Deassert Time

Parameter	MSA		Measurement	
Mask Deassert Time	≤ 100	ms	< 8	ms

Table 14: Mask Deassert Time

5.3.7 Other Timings

- LP Mode
- Application or rate Select
- Power Override or Power Set

Our modules do not provide these features and therefore these timings are N/A

5.4 I/O Timing for Squelch and Disable

5.4.1 Squelch Assert Time

In Fig 14 the results for switching off the Tx input signal is shown. As described earlier, due to the loop back configuration, this shows at the same time the Rx squelch behavior.

Tx Squelch is not implemented.

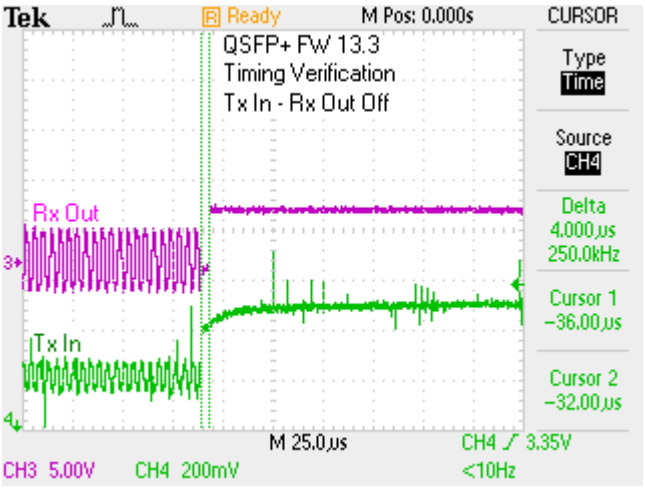


Fig 14 Rx Squelch Assert Time

Parameter	MSA		Measurement	
Rx Squelch Assert Time	≤ 80	µs	< 10	µs

Table 15: Rx Squelch Assert Time

5.4.2 Squelch Deassert Time

Also here, the loop back configuration shows Tx and Rx behavior in the same measurement.

The trigger shows when the Tx signal is switched on.

The Rx yields an output signal after less than 10 µs.

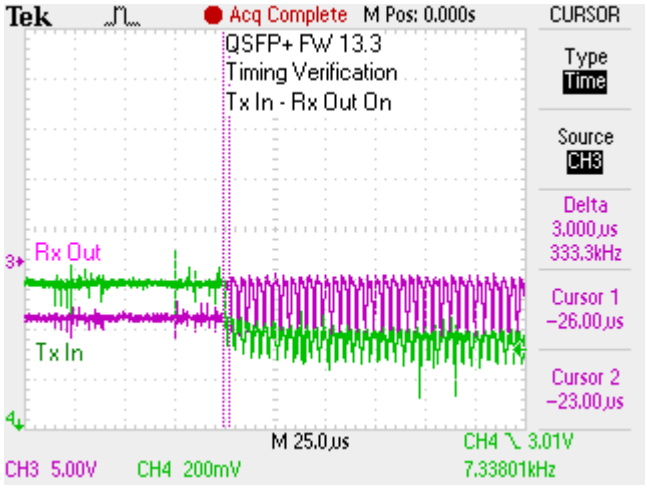


Fig 15 Rx Squelch Deassert Time

Parameter	MSA		Measurement	
Rx Squelch Deassert Time	≤ 80	µs	< 10	µs
Tx Squelch Deassert Time	≤ 400	ms	< 10	µs

Table 16: Rx and Tx Squelch Assert Time

5.4.3 Tx Disable Assert Time

As stated in 5.3.5, memory changes such as setting channel control bits are processed from the main loop within approx 10 ms after the memory location has been written.

The effect of dis- or enabling a Tx channel is monitored on the Rx output signal in the loop back configuration.

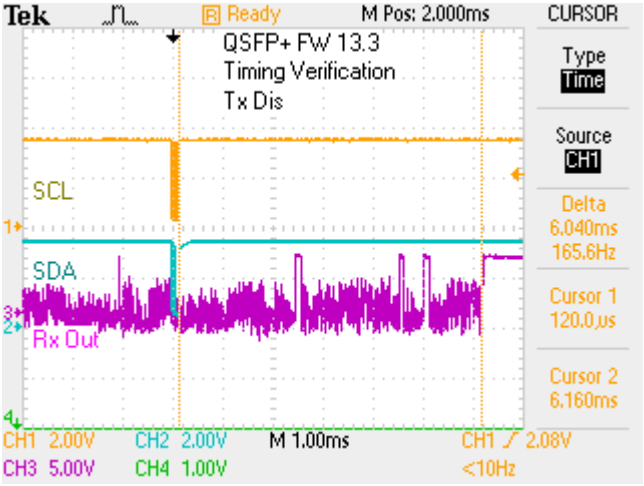


Fig 16 Tx Disable Assert Time

Parameter	MSA		Measurement	
Tx Disable Assert Time	≤ 100	ms	< 8	ms

Table 17: Tx Disable Assert Time

5.4.4 Tx Disable Deassert Time

As in 5.4.3, the loop back configuration shows the time of interest in the reappearance of the Rx output signal.

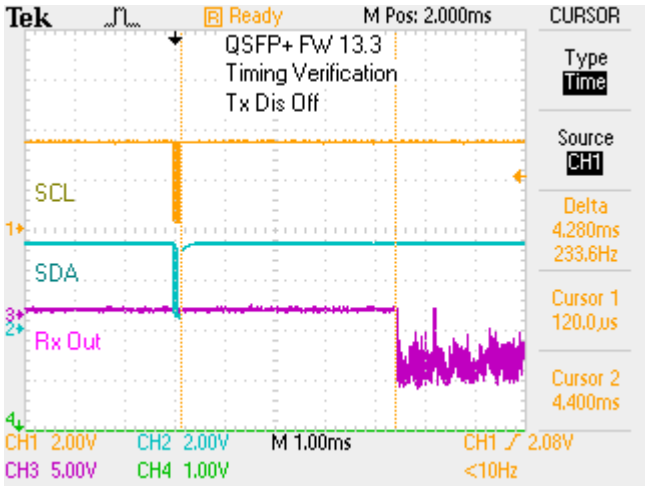


Fig 17 Tx Disable Deassert Time

Parameter	MSA		Measurement	
Tx Disable Deassert Time	≤ 400	ms	< 8	ms

Table 18: Tx Disable Deassert Time

5.4.5 Rx Output Disable Assert Time

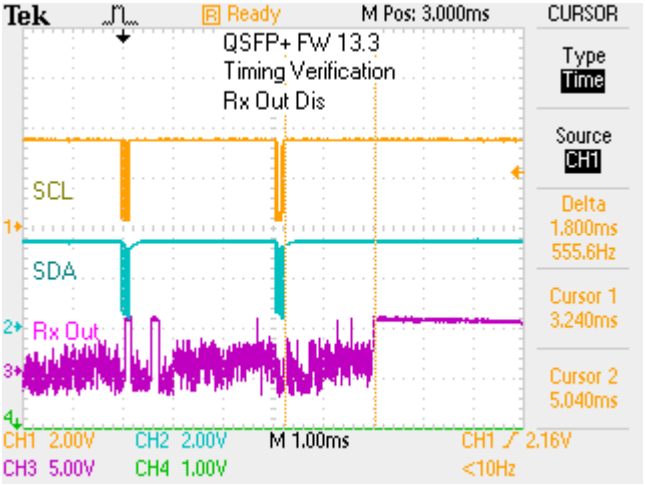


Fig 18 Rx Output Disable Assert Time

Parameter	MSA		Measurement	
Rx Output Disable Assert Time	≤ 100	ms	< 8	ms

Table 19: Tx Disable Deassert Time

5.4.6 Rx Output Disable Deassert Time

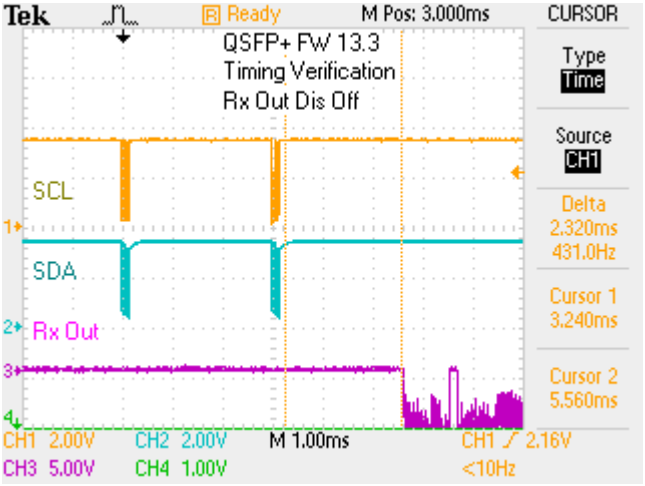


Fig 19 Rx Output Disable Deassert Time

Parameter	MSA		Measurement	
Rx Output Disable Deassert Time	≤ 100	ms	< 8	ms

Table 20: Tx Disable Deassert Time

5.4.7 Squelch Disable Assert Time

Like in 5.4.3 to 5.4.6, processing of memory write actions from the main loop is responsible for response time on these actions.

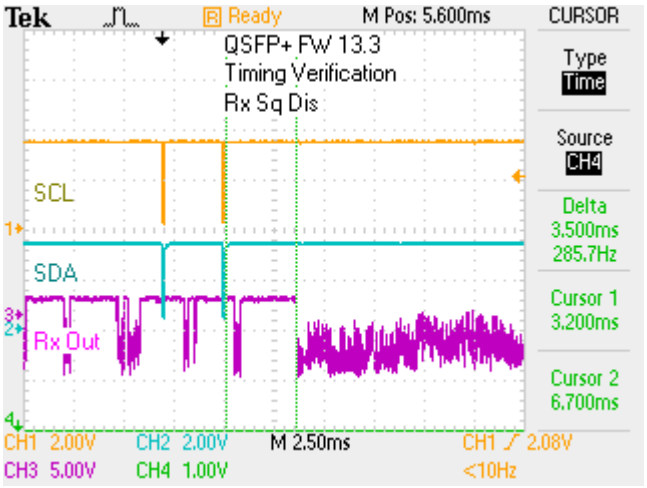


Fig 20 Rx Squelch Disable Assert Time

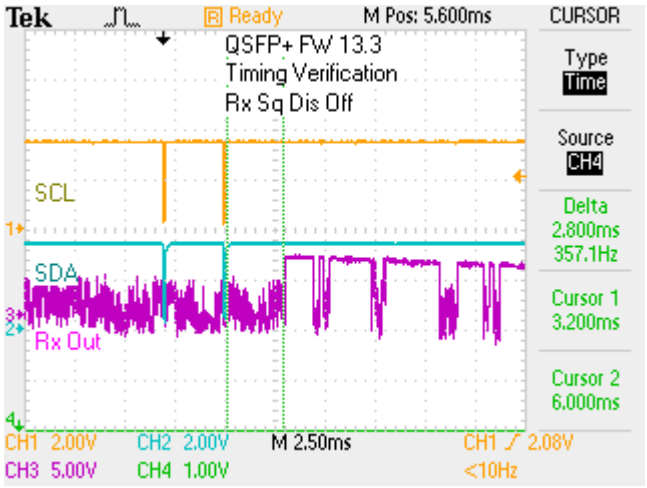


Fig 21 Rx Squelch Disable Deassert Time

Parameter	MSA		Measurement	
Squelch Disable Assert Time	≤ 100	ms	< 8	ms
Squelch Disable Deassert Time	≤ 100	ms	< 8	ms

Table 21: Squelch Disable Assert and Deassert Time