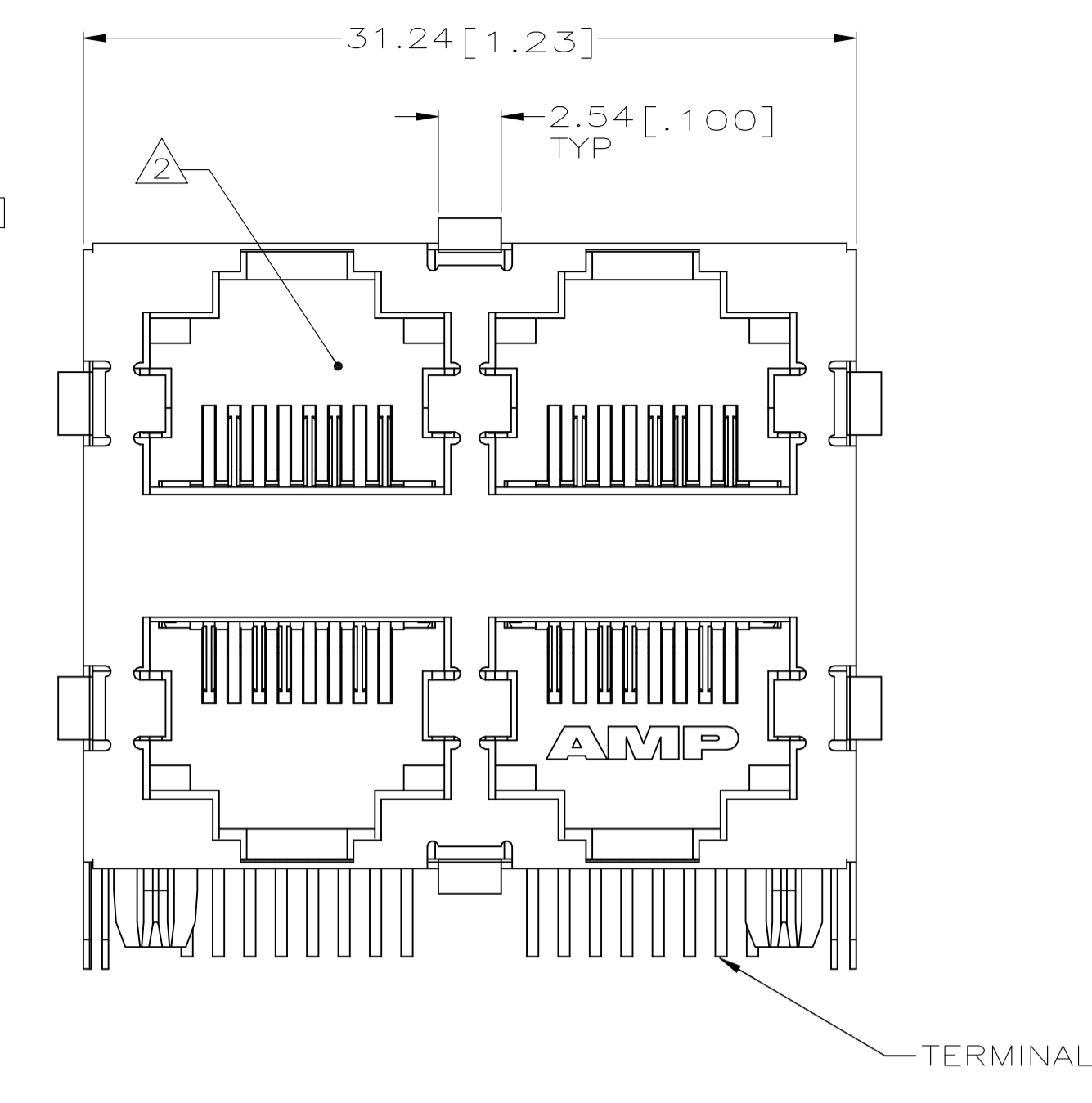
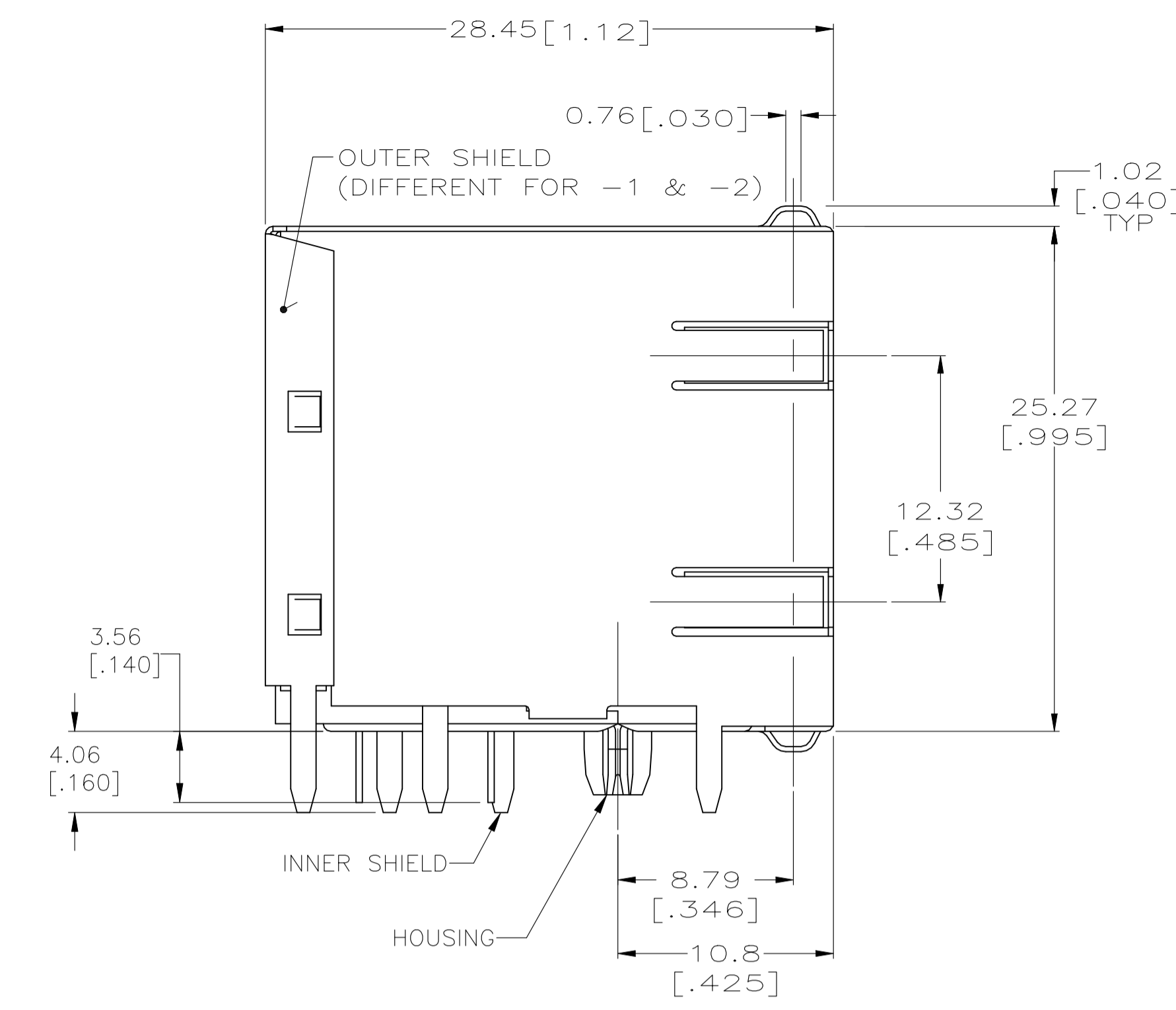
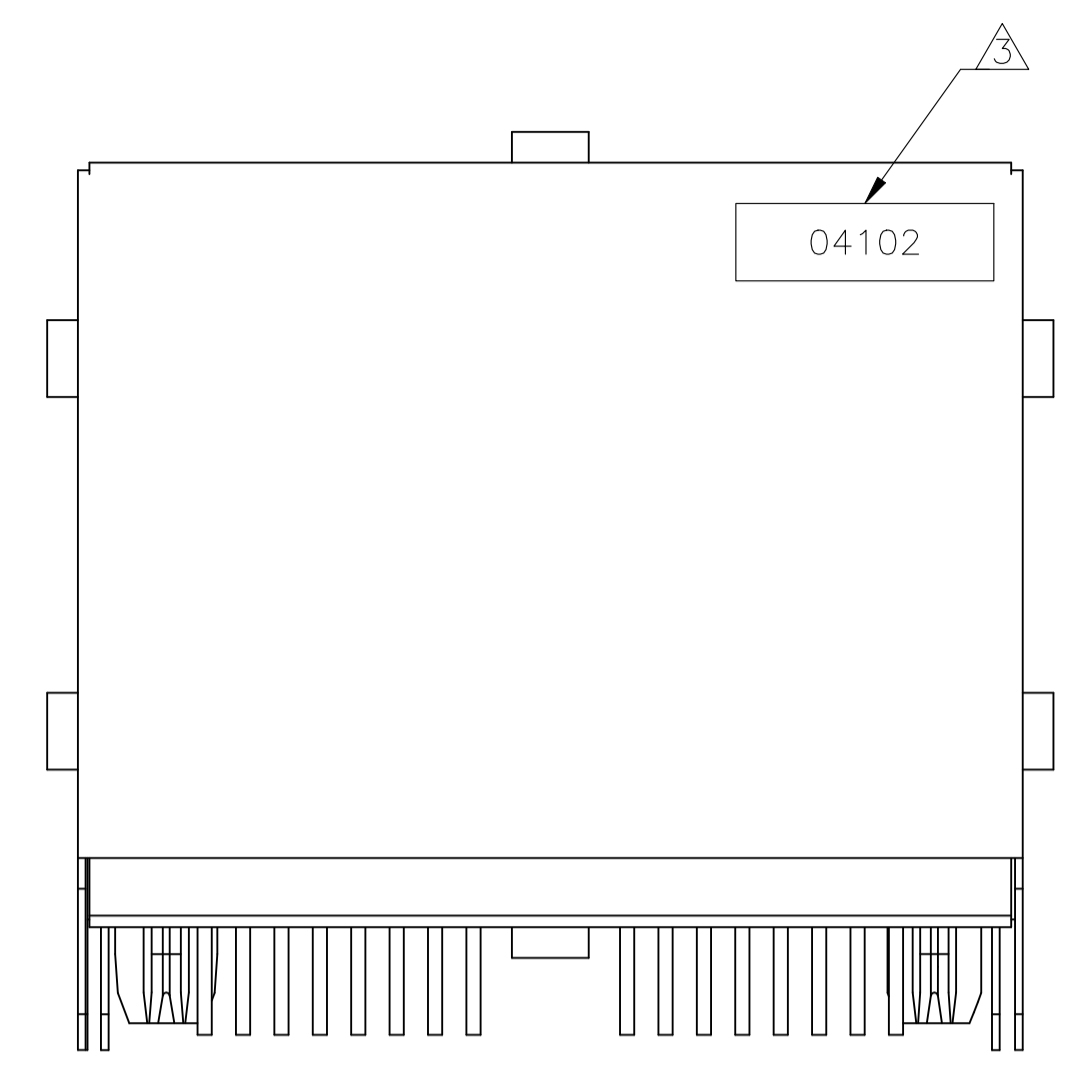
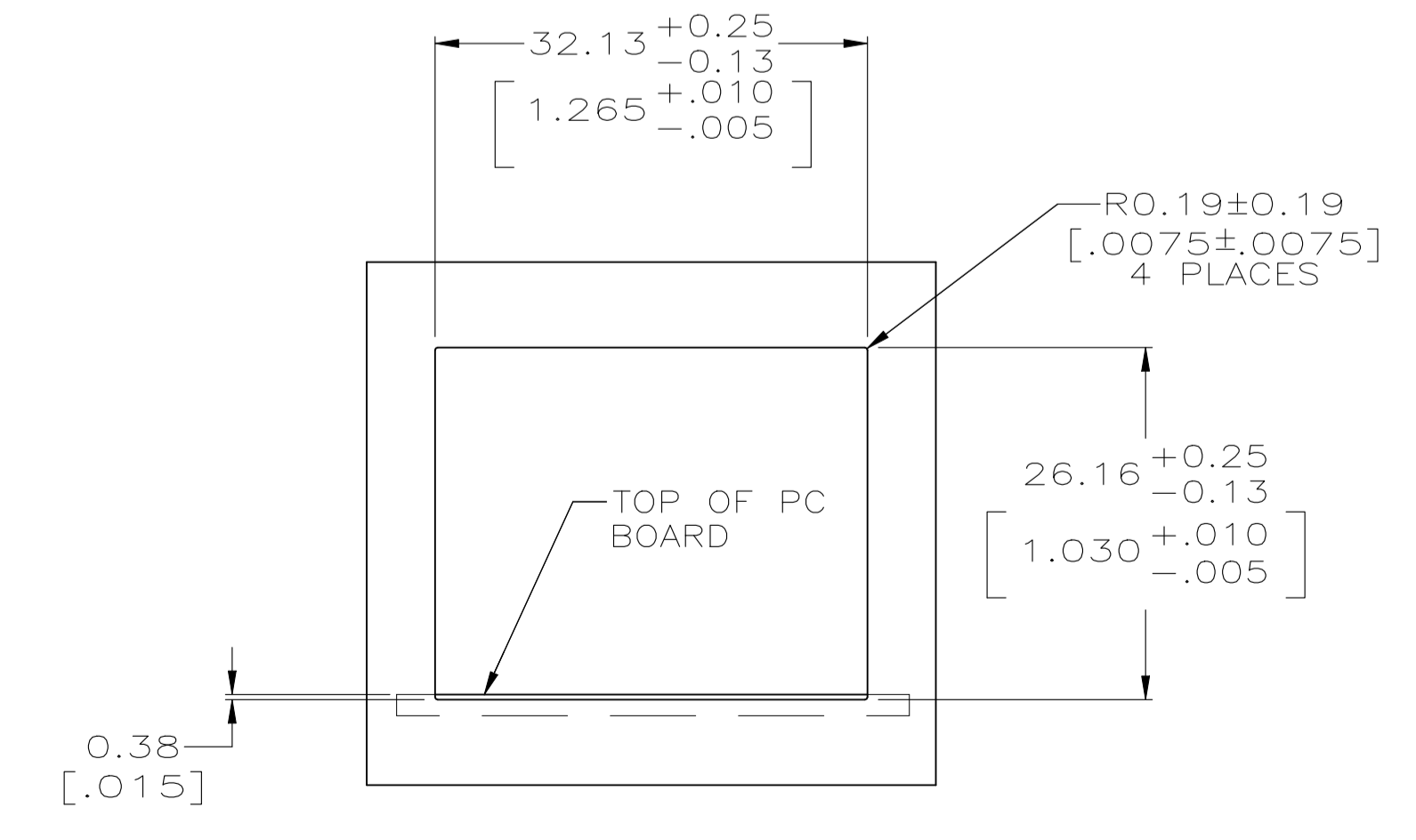
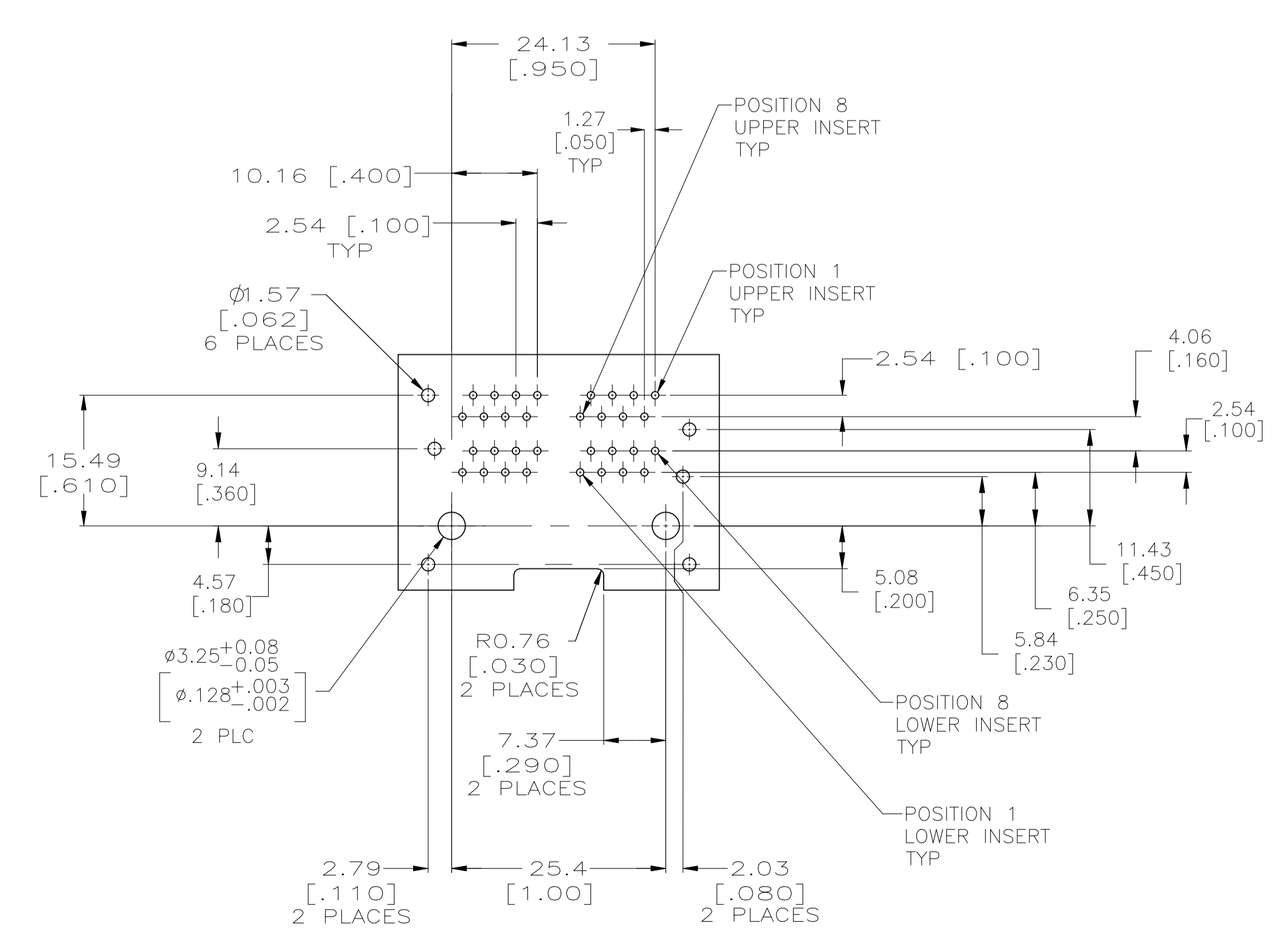
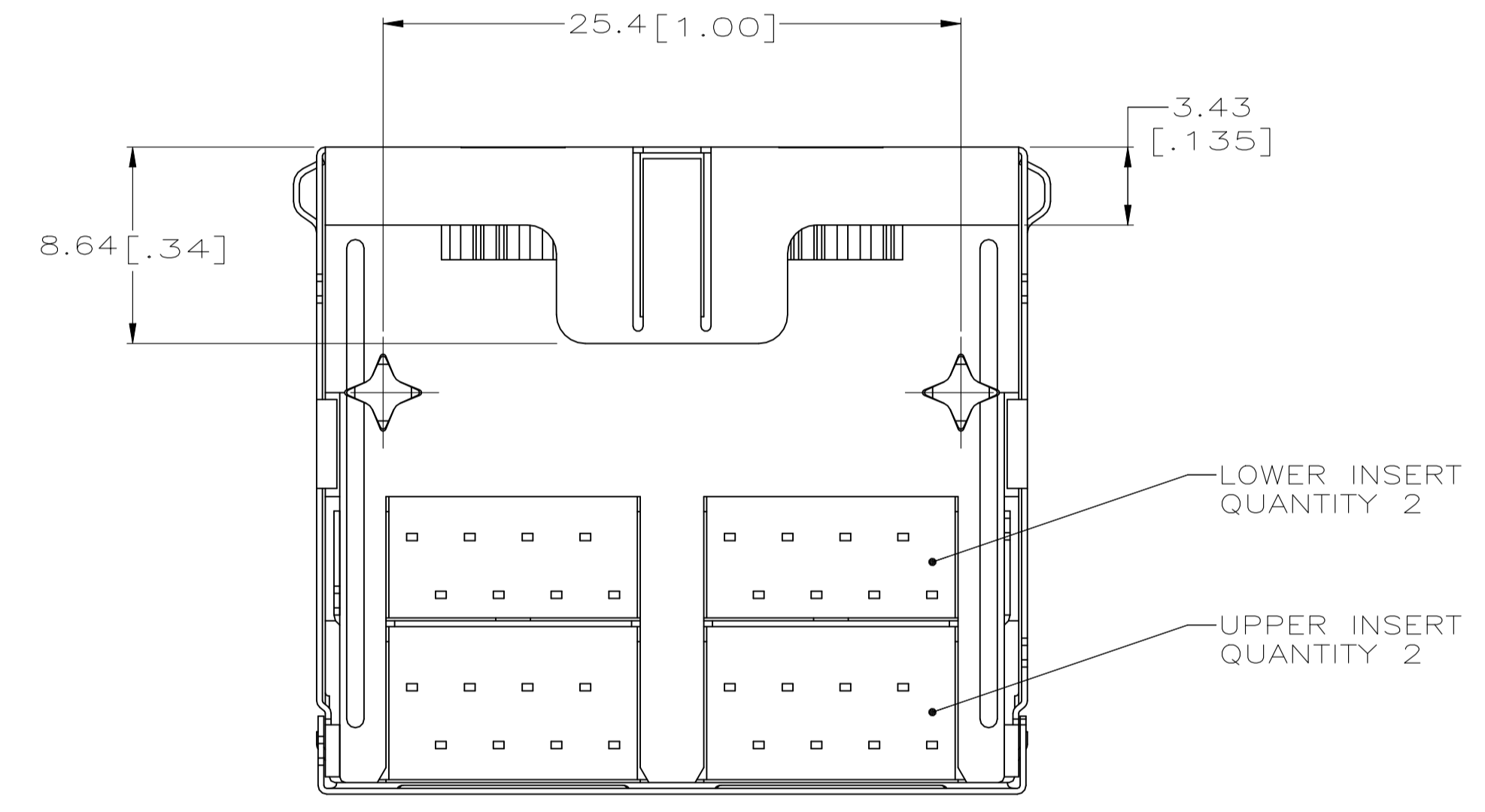


REVISIONS				
REV	DATE	DESCRIPTION	BY	APP'D
D1	31MAR2023	MODIFIED AS PER ECR-23-169440	KV	HW



- MATERIAL:
HOUSING - PCT POLYESTER, BLACK, UL94V-0.
OVERMOLDED TERMINAL ARRAY - HIGH TEMPERATURE NYLON, COLOR: NATURAL
TERMINALS - 0.33 [.013] THICK PHOS BRONZE PLATED WITH 1.27um [.000050] MIN THICK HARD GOLD IN LOCALIZED AREA AND 3.81um [.000150] MIN THICK MATTE TIN IN SOLDER AREA OVER 1.27um [.000050] MIN THICK NICKEL UNDERPLATE.
OUTER SHIELD AND INNER SHIELD - 0.25 [.010] THICK COPPER ALLOY PLATED WITH 1.27um [.000050] MIN THICK NICKEL. PCB GROUND TABS DIPPED WITH 2.03um [.000080] MIN TIN
- JACK CAVITY CONFORMS TO FCC RULES AND REGULATIONS, PART 68 SUBPART F.
- DATE CODE LOCATED ON REAR OF PART APPROXIMATELY AS SHOWN:
FIRST 2 DIGITS ARE LAST 2 DIGITS OF YEAR, SECOND 2 DIGITS ARE MANUFACTURING WORK WEEK, LAST DIGIT IS DAY OF WEEK, WITH SUNDAY = 1.
- PARTS PACKAGED IN SEALED BAGS WITH DESICCANT
- PARTS SUITABLE FOR LEAD FREE REFLOW PROCESSING TO 260° C



PC BOARD LAYOUT VIEWED FROM COMPONENT SIDE
SCALE 2:1

SUGGESTED PANEL CUTOUT DIMENSIONS
SCALE 2:1

THIS DRAWING IS A CONTROLLED DOCUMENT.		DIN A FERNANDEZ/L.A.M 07AUG2007		TE Connectivity	
DIMENSIONS: mm [INCHES]		CIR J. WESTMAN 07AUG2007			
TOLERANCES UNLESS OTHERWISE SPECIFIED:		APP'D S. FLICKINGER 07AUG2007		NAME STACKED MODULAR JACK ASSEMBLY, 2x2 PORT, 8 POSITION, SHIELDED, PANEL GROUND, CATEGORY 5, GIGABIT ETHERNET	
0 PLC ± -		PRODUCT SPEC		APPLICATION SPEC	
1 PLC ± -		SIZE		114-2048	
2 PLC ± 0.25(.01)		SCALE		A1 00779 C=2007104	
3 PLC ± 0.13(.005)		WEIGHT		0.000000	
4 PLC ± -		CUSTOMER DRAWING		SCALE 4:1 SHEET 1 of 1 REV D1	