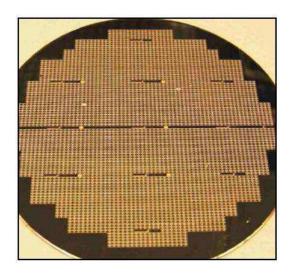
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# 12ch and 4ch 10G VCSEL Array Die

2156038-4, 2156038-2



#### **Features**

 850 nm oxide-confined Vertical-Cavity Surface-

Emitting Laser (VCSEL) die.

- 4 and 12 channels at 250 □m pitch.
- -10 °C to +85 °C operating temperature range.
- Fully passivated chip, hermetic packaging not required.
- Individual top side anode and cathodes pads.
- Top side contacts have minimum 3 □m Au for ease of bonding on the 100x130 □m pads.
- Backside common cathode is metalized with

suitable for mounting with thermal adhesive technology such as silver epoxy.

· Low relative intensity noise (RIN)

#### **Applications**

- QSFP (x4), CXP and CFP (x12) form factors
- Infiniband SDR (2.5G), DDR (5G) and QDR (10G)
- 40/100 Gb Ethernet (Draft 1.0 IEEE 802.3ba)
- Proprietary parallel highspeed data communication interconnect

#### Wafer Reliability Qualification

All wafers are qualified by accelerated life tests.

#### Ordering Information

**2156038-2**, 12x10G VCSEL die in waffle tray **2156038-4**, 4x10G VCSEL die in waffle tray

-10 °C to +85 °C



#### **Description**

Tyco Electronic's 10 Gb/s oxide-confined VCSEL array is based on the same well-proven, highly-reliable VCSEL technology platform as the proven 2.5 Gb/s devices. The platform has been developed from the beginning with focus on reliability, efficiency and high speed capability. Achieving the required performance at the lowest current density has been one of the main goals of the development work. The device employs a very efficient active structure and a design with low parasitics. High speed performance is achieved at a relative low bias above threshold.

The 2156038-2 and 2156038-4 are 850-nm VCSEL top contact array dies with coplanar anode and cathode pads designed for applications including Infiniband 2.5, 5 and 10 Gb/s in QSFP, CXP and CFP form factors.

40/100 GbE, active optical cables, as well as general purpose optical communication applications. Reliability assurance is based on Telcordia GR-468-CORE and the implementation of 100% wafer probe testing. The part is compliant to the EU directive 2002/95/EC issued 27 January 2003 [RoHS].

#### Shipping

The VCSEL bare dies array ships in waffle pack.

Contact Tyco Electronic's Sales or Distributor for high volume options.

#### **Testing**

Individual arrays are 100% DC tested on wafer level.



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## **Absolute Maximum Ratings**

Functional operation is not guaranteed under these conditions. Exceeding these ratings may cause permanent damage. (Note limits need not necessarily be applied together).

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T <sub>stg</sub>	-40	125	°C
Junction Temperature	T <sub>j, max</sub>		150	°C
Processing Temperature <sup>1</sup>	T <sub>pr</sub>		350	°C
Maximum Continuous Forward Current, in Logical "1"	I <sub>FM,"1"</sub>		15	mA
Maximum Average Forward Current	I <sub>FM,Avg</sub>		12	mA
Reverse Voltage	$V_{RM}$		5	V

<sup>1.</sup> Max. 60 seconds, non operating.

## **Optical and Electrical Characteristics**

(Substrate temperature Ts = 25 °C unless otherwise stated)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test condition
Threshold Current, T <sub>S</sub> = 25 °C	I <sub>th 25</sub>	1.0	1.2	1.3	mA	T <sub>S</sub> = 25 °C
Threshold Current, T <sub>S</sub> = 85 °C	I <sub>th 85</sub>	1.6	1.8	2.1	mA	T <sub>S</sub> = 85 °C
Slope Efficiency, T <sub>S</sub> = 25 °C	η <sub>25</sub>	0.30	0.35	0.40	W/A	T <sub>S</sub> = 25 °C
Slope Efficiency, T <sub>S</sub> = 85 °C	η <sub>85</sub>	0.24	0.28	0.32	W/A	T <sub>S</sub> = 85 °C
Average Forward Current	I <sub>F,Avg</sub>		7		mA	T <sub>S</sub> = 60 °C
Forward Voltage	٧ <sub>F</sub>	1.9	2.0	2.3	٧	I <sub>F</sub> = 6 mA
Optical Power Variation in Array	$\Delta P_0$			10	%	I <sub>F</sub> = 6 mA
Center Wavelength	$\lambda_{\mathrm{C}}$	845	850	855	nm	I <sub>F</sub> = 6 mA
Relative Intensity Noise-OMA	RIN <sub>12OMA</sub>		-135	-130	dB/Hz	I <sub>F</sub> = 6 mA
Optical Rise Time <sup>1</sup> (20 - 80%)	t <sub>r</sub>		20	30	ps	
Optical Fall Time <sup>1</sup> (20 - 80%)	t <sub>f</sub>		35	45	ps	
Differential Resistance	R <sub>diff</sub>		50	65	Ω	I <sub>F</sub> = 6 mA
Beam Divergence	2θ		25	35	deg.	I <sub>F</sub> = 6 mA
Thermal Resistance	R <sub>th j-s</sub>		1.5		°C/mW	

<sup>1.</sup> I<sub>avg</sub> = 6 mA, ER = 6 dB, unfiltered.



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#### **DIE ATTACH GUIDELINES**

**Die attach**: Mount the common cathode using thermally and electrically conductive adhesive such as silver epoxy.

Wire bonding: Gold bond wire with 32  $\mu$ m (1.25 mil) diameter or less.

#### **APPLICATION GUIDELINES**

#### **ESD Handling and Laser Safety**





DANGER - Invisible laser radiation emits perpendicular to device surface when connected to power source or battery. Avoid direct exposure to beam. Potential eye hazard. The VCSEL die is sensitive to electrostatic discharges. When handling the device, precaution for ESD sensitive devices should be taken. These precautions include use of ESD protected work area with wrist straps, controlled work benches, floors and similar areas were the bare chip is handled.

#### **Die Sales Disclaimer**

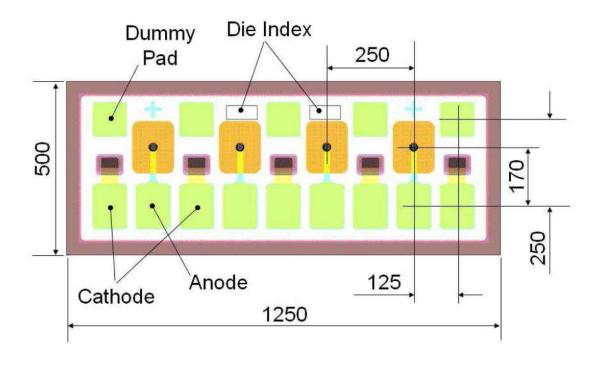
Tyco Electronic's has no control over the actions of parties involved in the [design] packaging or other processing or handling of die, and consequently Tyco Electronic's accepts no responsibility for the performance or functionality of the die or systems incorporating the die.

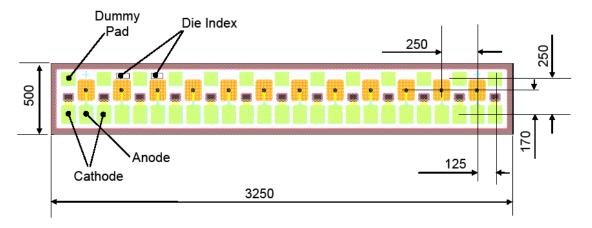
#### **Physical Properties**

Characteristic	Min.	Тур.	Max.	Unit	Comment
4 Channel Die Length	1230	1250	1270	μm	
4 Channel Die Width	480	500	520	μm	
12 Channel Die Length	3230	3250	3270	μm	
12 Channel Die Width	480	500	520	μm	
Die Thickness	190	200	210	μm	
Channel spacing	249	250	251	μm	
Bond-pad width		100		μm	
Bond-pad length		130		μm	
Bond-pad pitch		125		μm	

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# BARE DIE CHIP LAYOUT (4 and 12 channel respectively)



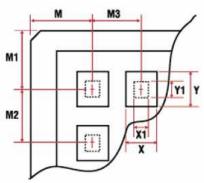


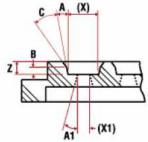
All dimensions in microns. "Dummy Pad" = not connected. "Die Index" = Unique Identification of Die on Wafer.



Chip Tray Material: Conductive Poly carbonate

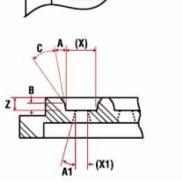
## Tray Dimensions for 12-ch and 4-ch bare dies respectively:



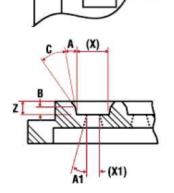


M1

M2



M3



#### POCKET LOCATIONS = 3.81mm ±0.08mm = 6.35mm ±0.08mm = 6.35mm ±0.05mm M2 = 2.54mm ±0.05mm МЗ = 18x7 (126) Array POCKET DETAILS X = 0.97mm ±0.05mm pocket size Υ = 4.32mm ±0.05mm pocket size Z = 0.43mm ±0.05mm pocket depth = 5° ±1/2° pocket draft angle No Cross Slots **OVERALL TRAY SIZE** = 50.80mm ±0.10mm = 3.96mm +0.05mm -0.08mm Flatness = 0.10mm

POCKET	LOCATIONS
М	= 4.32mm ±0.08mm
M1	= 4.11mm ±0.08mm
M2	= 2.24mm ±0.05mm
M3	= 2.21mm ±0.05mm
Array	= 20x20 (400)

## POCKET DETAILS

	Arrein Con Volin (Anni 2002) (
Х	= 0.97mm ±0.05mm pocket size
Υ	= 1.45mm ±0.05mm pocket size
Z	= 0.43mm ±0.05mm pocket depth
А	= 7° ±1/2° pocket draft angle
	EDM Finish On Pocket Floor
	No Cross Slots

#### OVERALL TRAY SIZE

Size	=	50.80mm ±0.10mm
Height	=	3.96mm +0.05mm -0.08mm
Flatness	_	0.10mm