

Silicon PIN Limiter Diodes

**MA4L Series
V3**

Features

- Lower Insertion Loss and Noise Figure
- Higher Peak and Average Operating Power
- Various P1dB Compression Powers
- Lower Flat Leakage Power
- Reliable Silicon Nitride Passivation

Description and Applications

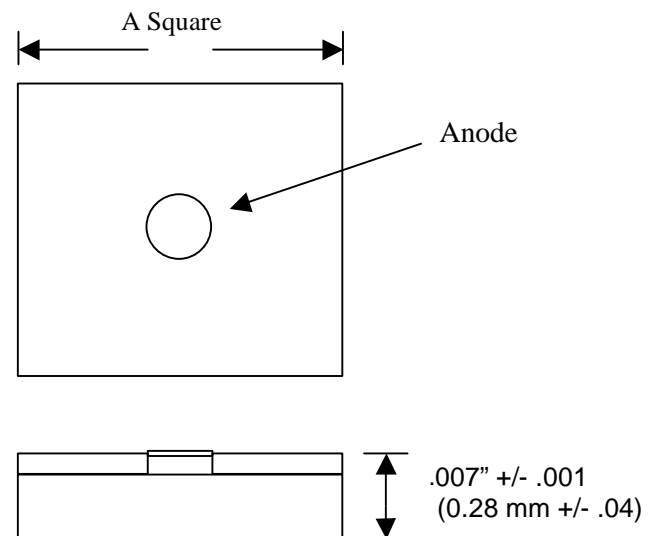
M/A-COM produces a series of small and medium I-region length silicon PIN diodes specifically designed for high signal limiter applications. Each of these devices provides circuit designers with lower insertion loss at zero bias, faster response and recovery times, and lower flat leakage power. This series of diode is available as passivated chips (ODS 132 or ODS 134) as well as hermetic surface mount and cylindrical ceramic packages. Consult factory for specific package style availability.

The MA4L Series of PIN limiter diodes are designed for use in passive limiter control circuits to protect sensitive receiver components such as low noise amplifiers (LNA), detectors, and mixers covering the 10MHz to 18GHz Frequency Band.

**Absolute Maximum Ratings¹
@ T_A = +25 °C (unless otherwise specified)**

Parameter	Absolute Maximum
Forward Current	100 mA
Operating Temperature	-55 °C to +125 °C
Storage Temperature	-55 °C to +150 °C
Junction Temperature	+175 °C
RF Peak Incident Power	Per Performance Table
RF C.W. Incident power	Per Performance Table
Mounting Temperature	+320°C for 10 seconds

1. Operation of this device above any one of these parameters may cause permanent damage.



ODS	Dimension	Mils	mm
132	A	15 +/- 2.0	0.59 +/- 0.04
134	A	20 +/- 2.0	0.79 +/- 0.04

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Un-Packaged Die Electrical Specifications @ + 25 °C

Part Number	Minimum Reverse Voltage @ -10µA (V)	Maximum Reverse Voltage @ -10µA (V)	Minimum C _{jov} @ 1 MHz (pF)	Maximum C _{jov} @ 1 MHz (pF)	Maximum R _{S10mA} @ 500 MHz (W)	Nominal Characteristics			
						Carrier Lifetime @ 10 mA (nS)	I-Region Thickness (µm)	Anode Contact Diameter (mils)	C.W. Thermal Resistance (°C/W)
MA4L022-134	20	35	0.13	0.23	2.0	10	2	1.0	175
MA4L032-134	30	50	0.13	0.20	1.8	15	3	1.4	150
MA4L101-134	100			0.15	2.0	90	13	3.5	50
MA4L401-132	250			0.30	1.2	800	25	4.5	35

Nominal High Signal Performance @ 25 °C

Part Number	Incident ³ Peak Power for 1 dB Limiting @ 9.4 GHz (dBm)	Incident ³ Peak Power for 10 dB Limiting @ 9.4 GHz (dBm)	Incident ³ Peak Power for 15 dB Limiting @ 9.4 GHz (dBm)	Recovery ³ Time, (3dB) @ 50 W Peak Power (nS)	Maximum ³ Incident Peak Power (dBm)	Maximum ⁴ CW Incident Power (dBm)
MA4L022-134	7	30	40	10	+49	+34
MA4L032-134	10	33	42	20	+50	+36
MA4L101-134	20	44	52	50	+54	+38
MA4L401-132	30	52	63	100	+63	+40

Notes for Specifications and Nominal High Signal Performance Table:

- 1. Maximum Series Resistance** - R_s, is measured at 500MHz in the ODS-30 package and is equivalent to the total diode resistance : R_s = R_j (Junction Resistance) + R_c (Ohmic Resistance)
- 2. Nominal C.W. Thermal Resistance** - θ_{TH} is measured in ceramic pill package, ODS-30, mounted to a metal (infinite) heatsink. Diode only thermal resistance values are approximately 2 °C/W lower in value than the ODS-30 listed package values.
- 3. Maximum High Signal Performance** – Measured using a single shunt diode (die) attached directly to the gold plated RF housing ground with 2 mil thick conductive silver epoxy in a 50Ω, SMA, connectorized test fixture. Chip anode contact is thermo sonically wire bonded using a 1 mil dia. gold wire onto a 7.2 mil thick Rogers 5880 duroid microstrip trace. A shunt coil provides the D.C. return. Test Frequency = 9.4 GHz, RF pulse width = 1.0 µS, 0.001 duty cycle.
- 4. Maximum C.W Incident Power** - Measured in a 50 Ω , SMA, connectorized housing @ 4GHz utilizing a TWT amplifier and the same single diode assembly configuration as stated in Note 3 above.

Die Handling and Mounting Information

Handling: All semiconductor chips should be handled with care in order to avoid damage or contamination from perspiration, salts, and skin oils. For individual die, the use of plastic tipped tweezers or vacuum pick up tools is strongly recommended. Bulk handling should ensure that abrasion and mechanical shock are minimized.

Die Attach: The die have Ti-Pt-Au back and anode metal, with a final gold thickness of 1.0 μm . Die can be mounted with a gold-tin, tin-lead eutectic solder preform or conductive silver epoxy. The metal RF and D.C. ground plane mounting surface requires solvent cleaning and a surface flatness of $< \pm 0.002''$.

Eutectic Die Attachment: An 80/20, gold-tin eutectic solder preform is recommended with a work surface temperature of 255°C and a tool tip temperature of 220°C. When the hot gas is applied, the temperature at the tool tip should be approximately 290°C. The chip should not be exposed to temperatures greater than 320°C for more than 10 seconds. Other solder types such as 60/40, tin-lead, may also be used.

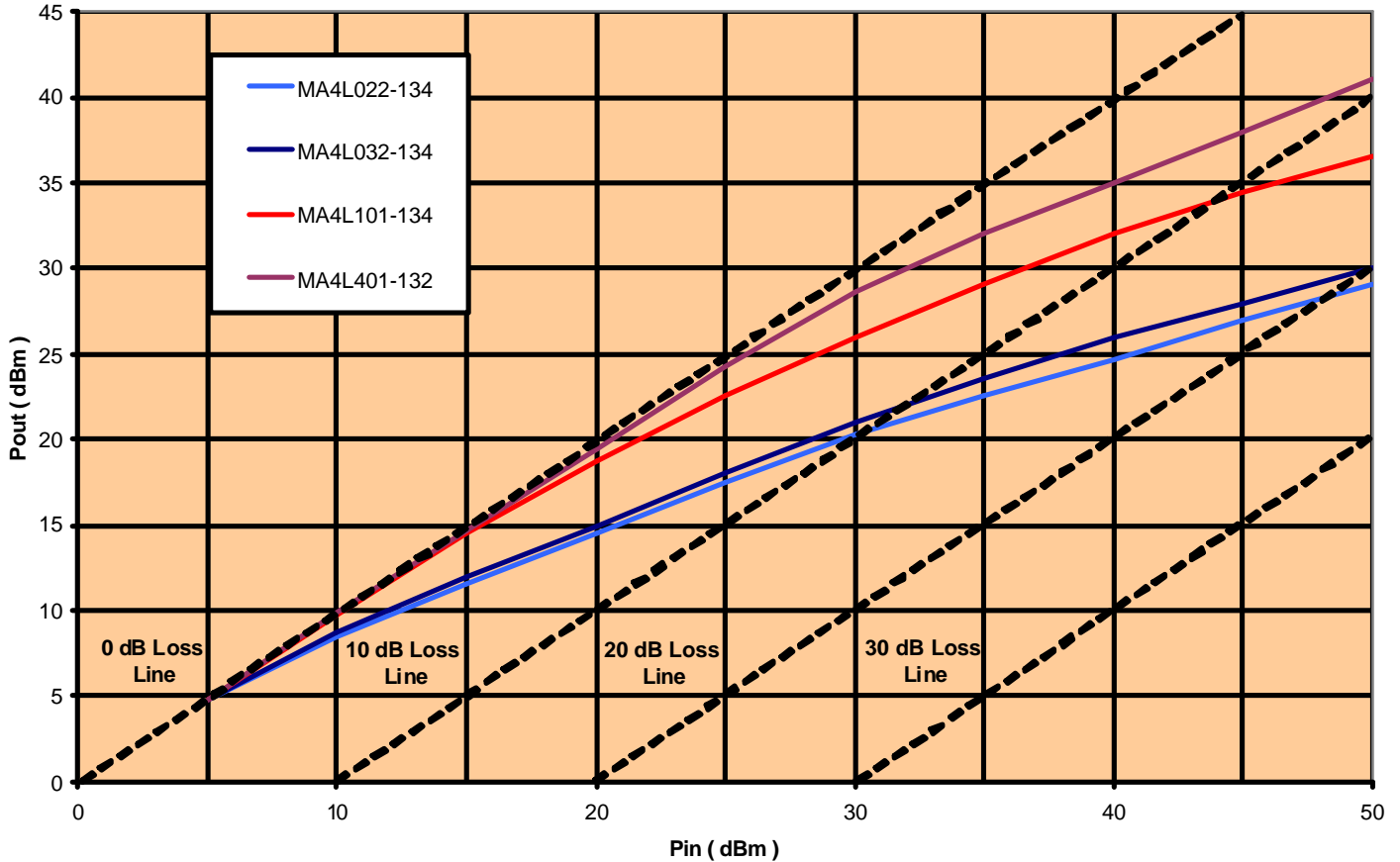
Epoxy Die Attachment: A thin, controlled amount of electrically conductive silver epoxy should be applied at approximately a 1–2 mils thickness to minimize ohmic and thermal resistances. A thin epoxy fillet should be visible around the perimeter of the chip after placement to ensure full area coverage. Cure conductive epoxy per manufacturer's schedule.

Die Bonding: The anode bond pads on these die have a Ti-Pt-Au metallization scheme, with a final gold thickness of 1.0 μm . Thermosonic wedge wire bonding of 0.001" diameter gold wire is recommended with a stage temperature of 150°C and a force of 18 to 40 grams. Ultrasonic energy should be adjusted to the minimum required. Automatic ball bonding can also be used.

See Application Note M541, "Bonding and Handling Procedures for Chip Diode Devices" for more detailed handling and assembly instructions at www.macom.com.

Typical High Signal Peak Power Performance for the Single Shunt Limiter Diode in a 50W Test Fixture (Note 3)

Typical Peak Power Performance for Single Shunt Limiter Diode in 50 Ohm System at 9.4 GHz, 1uS Pulse Width, 0.001 Duty

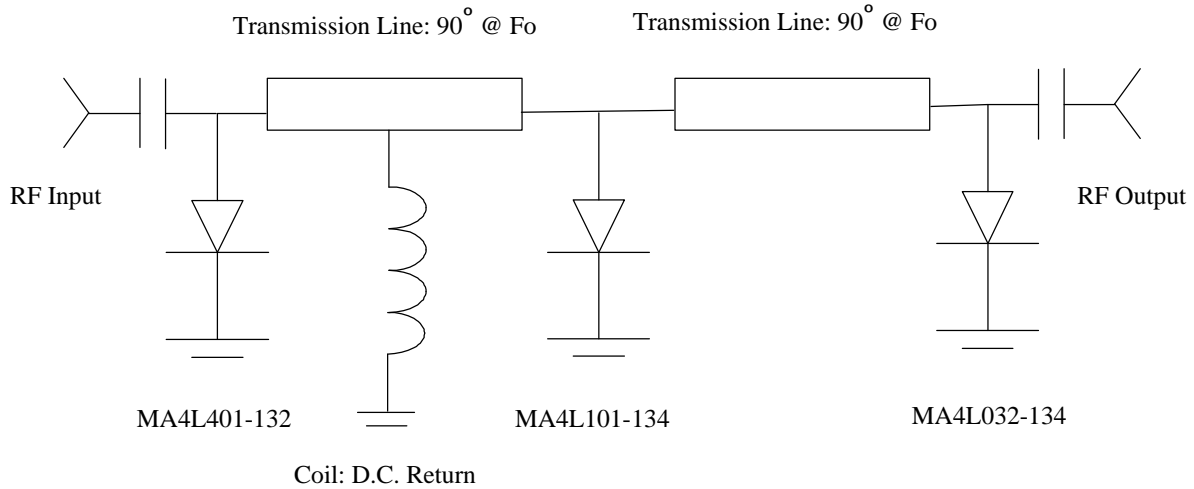


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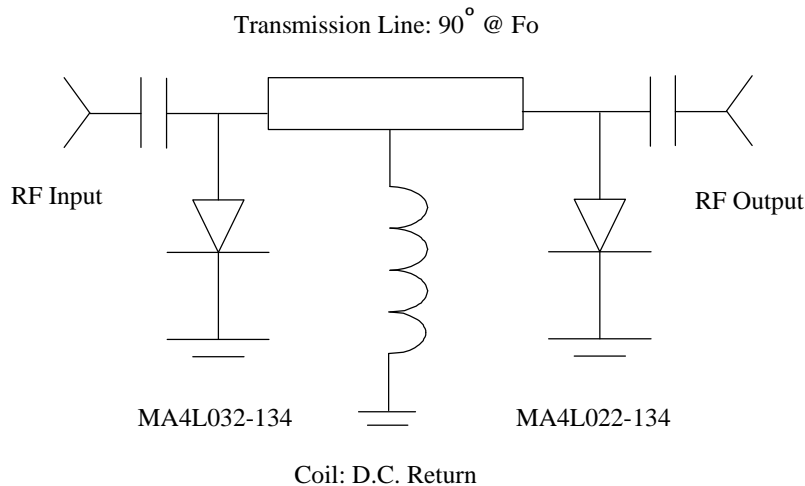
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Application Circuits

Typical +60dBm Peak Power, 1mS P.W., 0.001% Duty Cycle, +20 dBm Flat Leakage Limiter Circuit



Typical +50 dBm Peak Power, 1mS P.W., 0.001% Duty Cycle, +20 dBm Flat Leakage Limiter Circuit



Popular Case Styles and Associated Parasitics (Table 1)

Package Style	Package Type	Cpkg (pF)	Ls (nH)
30	Ceramic Pill	0.18	0.60
31	Ceramic Pill	0.18	0.60
32	Ceramic Pill	0.30	0.40
36	Ceramic Pill	0.18	0.60
137	Ceramic Surface Mount with Leads	0.14	0.70
186	Ceramic Surface Mount with Leads	0.18	0.70
1056	Ceramic Surface Mount with Wrap Around Contacts	0.20	0.70

Part Numbering and Ordering Information

1. The die only P/N's use either the -132 or -134 suffix (see Electrical Specification Table).
2. The packaged P/N's use the associated suffix as defined in Table I instead of the die number.

For example, the MA4L032-134 die in the 186 style package becomes: MA4L032-186

Equivalent P/N Cross Reference

1. MA4L022 is the diode circuit equivalent and functionally identical to the MA4L011 and MA4L021.
2. MA4L032 is the diode circuit equivalent and functionally identical to the MA4L031.