NOTE

All numerical values are in metric units [with U.S. customary units in brackets]. Dimensions are in millimeters [and inches]. Unless otherwise specified, dimensions have a tolerance of ±0.13 [±.005] and angles have a tolerance of ±2°. Figures and illustrations are for identification only and are not drawn to scale.

1. INTRODUCTION

This specification covers recommendations for application of Gigabit Ethernet Multimode SFF MT-RJ Transceivers. The transceiver is an 850 nm vertical cavity surface emitting laser-based (VCSEL) fiber optic device used primarily in Gigabit Ethernet applications. A type MT-RJ connector is provided as the external connector on the optical interface. Gigabit Ethernet can be transmitted and received by these transceivers over a pair of 62.5 µm or 50 µm core multimode optical fibers. The transceiver operates from a single +3.3 Vdc power supply and contains DC coupled transmitter and receiver sections that have positive emitter coupled logic/low voltage positive emitter coupled logic (PECL/LVPECL) compatible data interfaces. Although these transceivers have been specifically designed and tested to meet certain standards, the transceivers can also be used for Fibre Channel applications.

The transceiver (or module) is for use in the network to cable plant interface. The package style is per the Small Form Factor (SFF) Multi-Source Agreement (MSA) with an MT-RJ interface connector.

The transceiver features an EMI gasket to provide electrical contact to the bezel. The housing and case grounds minimize electromagnetic interference (EMI) susceptibility and radiated emissions.

When corresponding with Tyco Electronics Personnel, use the terminology provided in this specification to facilitate your inquiries for information. Basic terms and features of this product are provided in Figure 1.

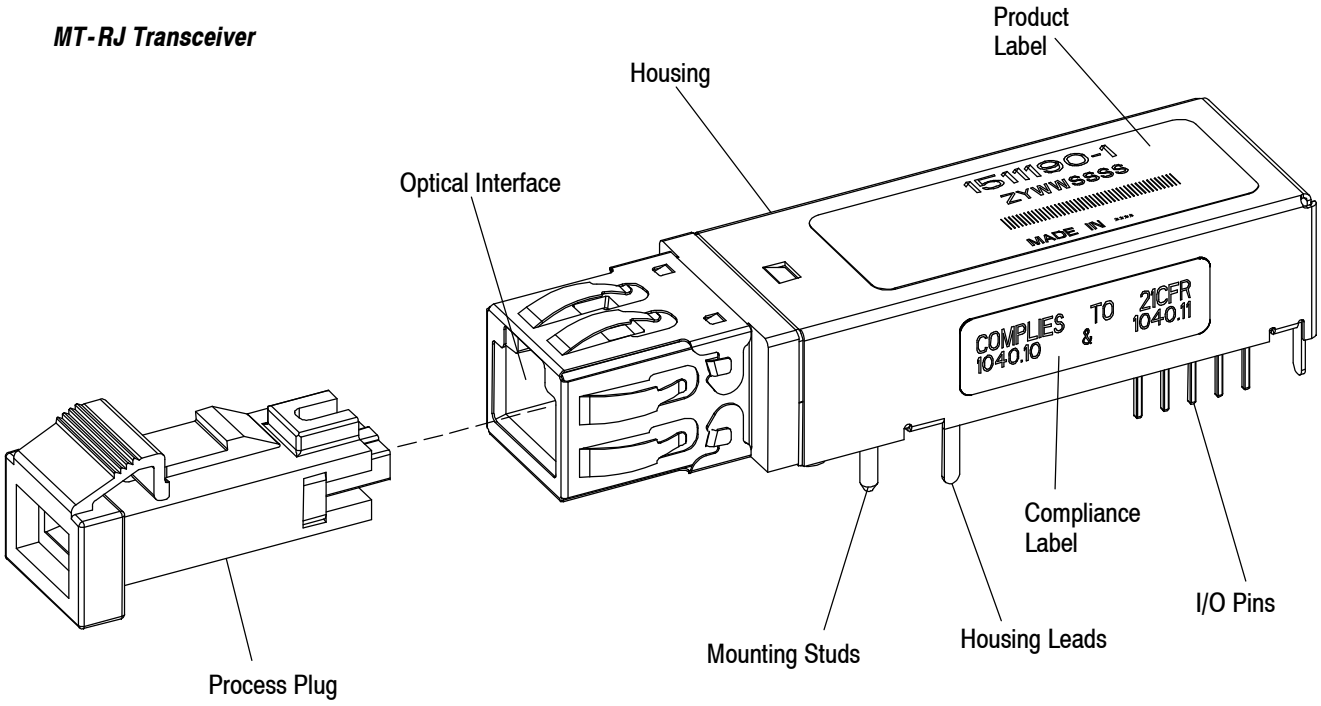


Figure 1

2. REFERENCE MATERIAL

2.1. Revision Summary

- Updated document to corporate requirements
- New logo and format

2.2. Customer Assistance

Reference Product Base Part Number 1511190 and Product Code A459 are representative of Gigabit Ethernet multimode SFF MT-RJ Transceivers. Use of these numbers will identify the product line and expedite your inquiries through a service network established to help you obtain product and tooling information. Such information can be obtained through a Tyco Electronics Representative or, after purchase, by calling Product Information at the number at the bottom of page 1.

2.3. Drawings

Customer Drawings for product part numbers are available from the service network. If there is a conflict between the information contained in the Customer Drawings and this specification or with any other technical documentation supplied, call Product Information at the number at the bottom of page 1.

2.4. Specifications

Design Objective 108-2179 provides expected product performance and test information.

2.5. Catalogs

Sales Catalogs available are 1654858 (Gigabit Ethernet Multimode SFF MT-RJ Transceivers) and 1307895 (Fiber Optic Product Catalog).

2.6. Standards and Publications

Standards and publications developed by the Institute of Electrical and Electronic Engineers, Inc. (IEEE), American National Standards Institute (ANSI), Telecommunications Industry Association and Electronic Industries Alliance (TIA/EIA), International Electrotechnical Commission (IEC), and Food and Drug Administration (FDA) provide industry test and performance requirements. Documents available which pertain to this product are:

IEEE Std. 802.3, Clause 38, “Physical Medium Dependent (PMD) Sublayer and Baseband Medium, Type 1000BASE-Long Wavelength Laser (LX) and 1000BASE-Short Wavelength Laser (SX)”

NOTE

Although these transceivers have been specifically designed and tested to meet this standard, the transceivers can also be used for Fibre Channel applications.

IEEE Std. 802 Annex 36A, “Jitter Test Patterns”

ANSI X3.230, “Information Technology-Fibre Channel-Physical and Signaling Interface (FC-PH)”

TIA/EIA-455-95, “Absolute Optical Power Test for Optical Fibers and Cables”

TIA/EIA-526-4, “Optical Eye Pattern Measurement Procedure”

TIA/EIA-526-14, “Optical Power Loss Measurements of Installed Multimode Fiber Cable Plant—OFSTP 14A”

TIA/EIA-455-107, “FOTP 107—Determination of Component Reflectance or Link/System Return Loss using a Loss Test Set”

IEC 60825-1, “Part 1: Safety of Laser Products—Equipment Classification, Requirements and User’s Guide”

IEC 60825-2, “Part 2: Safety of Optical Fiber Communication Systems”

FDA 21 Code of Federal Regulations (CFR) Chapter 1, Part 1040, “Performance Standards for Light Emitting Products”

NOTE

All products that contain a laser must comply with government regulations for laser safety. In the U.S., the applicable standard is FDA 21 CFR Chapter 1, Part 1040, and outside the U.S., IEC 60825-1 applies. These transceivers are designed and tested to meet the requirements of these standards and found to be in compliance with Class 1 laser safety limits. When operated within the limits specified in this document, this product conforms to IEC 60825-1: 1993 +A1: 1997 +A2: 2001, Class 1 laser product requirements.

2.7. Application Notes

ON SEMICONDUCTOR AN1406/D, Sept., 1999: Rev 2, “Designing with PECL (ECL at +5.0 V)—The High Speed Solution for the CMOS/TTL Designer.” Cleon Petty and Todd Person at Semiconductor Components Industries, LLC (http://www.onsemi.com/pub/Collateral/AN1406-D.PDF)

ON SEMICONDUCTOR AN1672/D, May, 2001: Rev 3, “The ECL Translator Guide—ECL, TTL, PECL, LVECL, LVPECL, CMOS, LVTTL, How to Make Them Talk to Each Other.” Paul Stockman and Paul Hunt at Semiconductor Components Industries, LLC (http://www.onsemi.com/pub/Collateral/AN1672-D.PDF)

2.8. Miscellaneous

Motorola DL140/D, “High Performance ECL Data Book, ECLinPs and ECLinPS Lite,” provides a comprehensive description of transmission line design and termination techniques.

SFF Multi-Source Agreement (MSA)—The package for the transceiver has been designed to fully comply with the SFF MSA (http://www.schelto.com/SFF/index.html)

3. REQUIREMENTS

Use of controls on this product, adjustments made to this product, or performing procedures other than those specified in this document, may result in exposure to hazardous radiation.

3.1. Laser Safety

These transceivers are designed and tested to be in compliance with Class 1 laser safety standards both in the U.S. and internationally when used within the limits specified in this document for temperature and power supply. These products are inherently safe since prolonged exposure to radiation from such lasers will not cause damage to the skin or eyes.

Laser safety is maintained during normal operation through factory-set adjustments which compensate for the known light of the laser versus current behavior as a function of temperature and power supply voltage. During single point failure conditions, laser safety is preserved by the internal optical subassembly which limits the emitted optical signal and ensures that even at the maximum light output of the VCSEL, the accessible emission will not exceed Class 1 limits.

3.2. Storage

A. Ultraviolet Light

Prolonged exposure to ultraviolet light may deteriorate the chemical composition used in the transceiver material.

B. Shelf Life

The transceivers should remain in the shipping containers until ready for use to prevent deformation. The transceivers should be used on a first in, first out basis to avoid storage contamination that could adversely affect performance.

Do not stack product shipping containers too high that the containers will buckle or deform.

C. Chemical Exposure

Do not store transceivers near any chemical listed below as they may cause stress corrosion cracking.

Alkalies	Ammonia	Citrates	Phosphates Citrates	Sulfur Compounds
Amines	Carbonates	Nitrites	Sulfur Nitrites	Tartrates

3.3. Assembly Precautions

Personnel handling these transceivers or printed circuit (pc) boards containing these transceivers must observe the following precautions during assembly and testing procedures:

- Electrostatic discharge (ESD) precautions consistent with Class 1C per ESD STM5.1-1998 (1000 volts to <2000 volts) are required.
- Multiple mating test fixtures should be designed such that the connector ferrules have sufficient alignment float when inserted into the transceivers. An overly rigid, blind mating test fixture may damage the transceivers, test fixture, or both when mating.

- Ferrules used in testers should be inspected, cleaned, and maintained regularly. Inspection should be performed under sufficient magnification to detect micro-cracks in the fiber. Dry, oil free, filtered compressed air or dry nitrogen is recommended for removing dust and debris from ferrules and interface of the transceivers before connection.

Soldering

These transceivers are through-hole devices. The recommended method for soldering the transceivers to the board is wave soldering. Vapor-phase and reflow surface-mount processes are not recommended. Pins can be soldered at 240°C for 10 seconds, provided the board adequately protects the case.

The recommended solder is a type S composition containing 60% tin. The recommended flux is a water-soluble white rosin, type S.

MT-RJ Gigabit Transceivers are supplied with process plugs that are inserted into the optical interface. The plugs protect the interface from contamination during soldering and cleaning. It is also a good idea to keep the plugs installed during shipping and handling to prevent dust and dirt from entering the interface. Although the plugs can emit air during a bubble leak test, this does not mean that the plugs leak and allow liquids or gases into the optical interface.

Cleaning and Drying

Boards should be cleaned with aqueous cleaners. Avoid solvents that could harm the polysulfone bodies of plastic-cased devices. The transceivers can be exposed to an air knife stream when being dried. On a drying rack, the optical interface should point down to ensure the best drainage away from the interface. If the plug is to be removed at this time, be careful not to allow water into the interface. Water can leave a residue on the optics that will degrade the optical performance characteristics.

3.4. Function

Like the 10 Mb/s ethernet and 100 Mb/s Fast Ethernet, Gigabit Ethernet functionality is grouped according to several distinct layers. The upper layers define the protocol and software operations necessary to allow Gigabit Ethernet local area networking hardware, such as switches and repeaters, to communicate with one another. The lower layers define the hardware operations and interface signals which allow the circuitry to function together seamlessly at the circuit board level.

The lowest layer is the physical layer (PHY). The PHY defines the interface between the data transmission device and the physical medium (optical fiber or copper wire) used to carry data from source to destination. The PHY is further divided into sublayers which include the physical coding sublayer (PC) (8b/10b encoding), the physical medium attachment sublayer (PMA) (serializer/deserializer and clock recovery), and the physical medium dependent sublayer (PMD) (850 nm optics, 1300 nm optics, or copper cable). This transceiver forms the heart of a 1000BASE-SX PHY. See Figure 2.

Gigabit Ethernet PHY

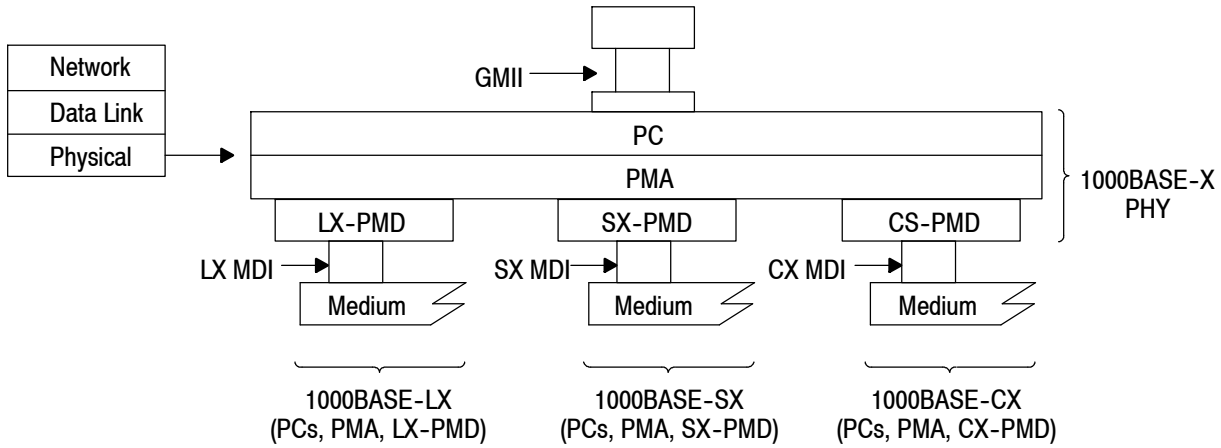


Figure 2

PHY sublayer partitioning at the circuit board level is left to the individual preference of the integrated circuit designers. In a real world system, the integrated circuit chips, fiber optic transceiver, cable plant, and connectors are combined to form a complete data communication link. A common approach to fiber optic transceiver-based PHY design is shown in Figure 3.

Typical Gigabit Ethernet Fiber Optic Transceiver-Based PHY

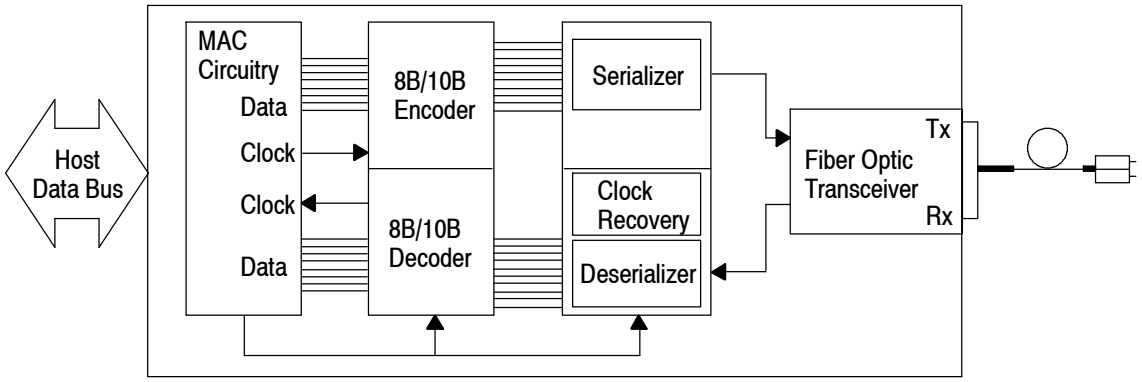


Figure 3

The transceiver consists of a transmitter and receiver for performing the electro–optic conversions between electrical PECL/LVPECL logic level signals and optical signals. The transmitter consists of an 850 nm VCSEL and a laser driver integrated circuit. The receiver contains a preamplifier with a GaAs PIN photodiode followed by a limiting amplifier with PECL/LVPECL compatible logic outputs. See Figure 4.

VCSELs provide several advantages over edge emitting lasers when used for high speed data transmission. VCSELs require low drive current for high optical power output which results in decreased heat dissipation in the transmitter circuit. VCSELs also exhibit well behaved circular beam characteristics which leads to simplified alignment between the laser and the optical fiber. Since VCSELs emit light from their surface, as opposed to their edge, they can be easily tested and screened at the wafer level. The same cannot be said for edge emitting devices which must be cleaved into individual die and placed on a submount before testing can be accomplished. A properly designed and manufactured VCSEL is inherently reliable and does not require the rigorous screening associated with high reliability lasers selected for use in data communication systems.

Transceiver Functional Block Diagram

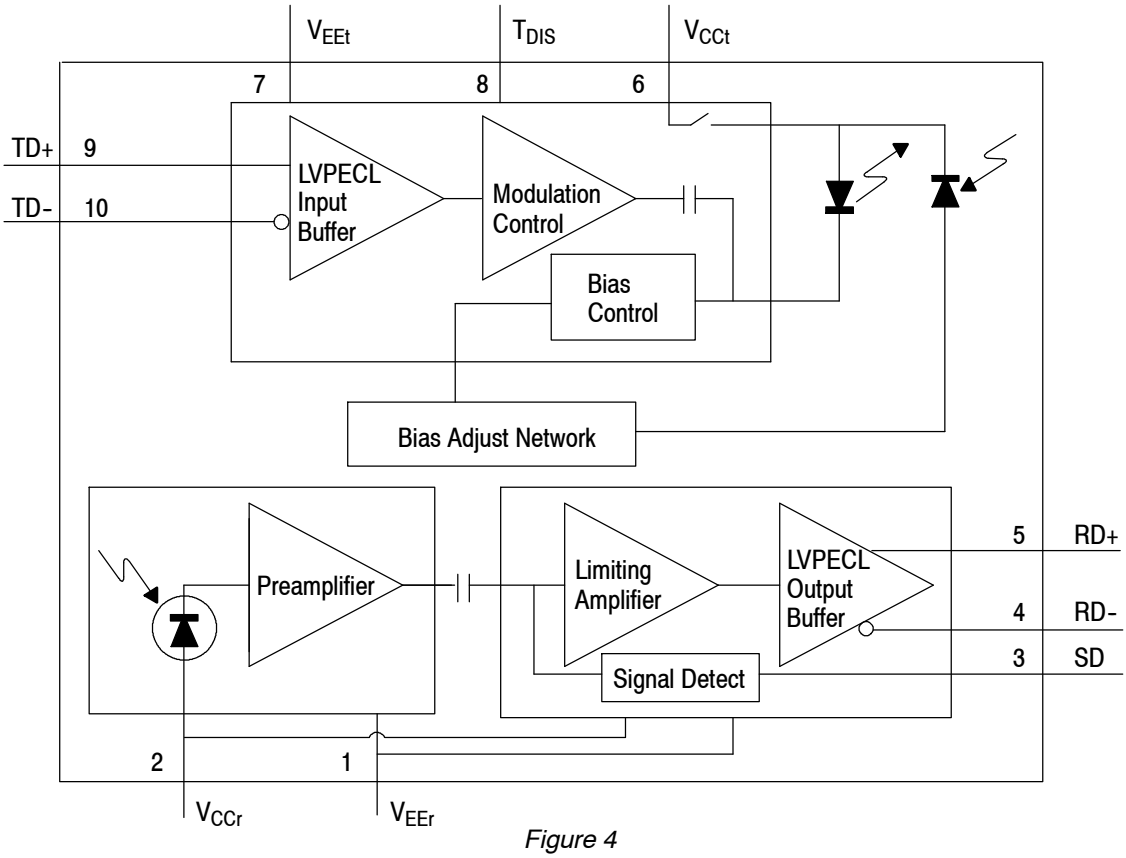


Figure 4

The laser driver circuit accepts a digital logic level (PECL/LVPECL) input and provides the proper bias and modulation currents for maintaining the VCSEL within its specified operating range. The receiver accepts an input from the fiber optic cable in the form of a modulated optical signal and converts it to a digital logic (PECL/LVPECL) output. This signal is focused onto a small area GaAs PIN photodiode which converts the incident light into a proportional photocurrent. The transimpedance preamplifier converts the photocurrent into an analog voltage which is fed to the limiting amplifier (also referred to as a quantizer). The limiting amplifier converts the analog voltage into a digital logic signal that interfaces with external circuitry, such as a PHY chip.

3.5. (Signal Detect) and Reference Generator

The signal detect (SD) circuit compares the signal from the quantizer with a reference generator to determine the presence of an optical signal. The signal is used as a rough link integrity monitor, not a bit error rate (BER) monitor. It is useful for recognizing when the input to the receiver has dropped well below recommended levels. The comparison is done with hysteresis so that the signal detect assert and deassert occur at different power levels. The difference between the assert and deassert levels provided by the hysteresis ensures chatter-free operation by preventing the signal from toggling between HIGH and LOW if the power levels hover around a certain point. The signal detect flag is a TTL signal and should be connected directly to the controller chip with no external biasing resistor present.

3.6. Transmitter Disable

This transceiver provides a laser transmitter disable input. The transmitter is constantly biased, so unmodulated light is sent across the fiber link even when no data is being transmitted. To prevent the possibility of a receiver inadvertently sensing a signal during a period when no data is transmitted, the transmitter can be disabled by connecting this transmitter disable input directly to an external controller. The transmitter disable input uses TTL logic levels. If the system designer does not wish to use the transmitter disable function, it can remain disconnected since an internal pull-down resistor is present to ensure the transmitter is always enabled.

3.7. Data Encoding and AC Coupling

Gigabit Ethernet PHY chips use an encoding scheme known as 8b/10b which is an advantageous way of transmitting data using fiber optic transceivers. This encoding limits the run length (the number of consecutive 1s or 0s) and maintains DC balance by ensuring that, over time, an equal number of 1s and 0s are sent through the link. This is refered to as disparity neutral or balanced data.

The receiver of the transceiver is internally AC coupled. Specifically, there are internal AC coupling capacitors in the data path between the preamplifier and post amplifier which control the lower 3 dB cutoff frequency of the receiver. This is done to limit the low frequency noise response of the receiver and improve sensitivity.

A direct result of AC coupling the receiver is that links, which use these transceivers, will not pass signals at DC or low frequencies. Long continuous strings of logic 1s or 0s, which have significant low frequency content, will be distorted by an AC coupled link. For this reason, the transceiver requires data to be encoded in a manner which limits the run length such as 8b/10b, asyschronous transfer mode/synchronous optical network (ATM/SONET) scrambling, etc. This is not a unique characteristic of these transceivers and is common for most commercially available Gigabit fiber optic transceivers.

The transceiver is provided with differential data inputs and outputs and these are both internally DC coupled. The transmitter input is internally terminated with a 100 ohm differential termination resistor and the receiver output requires that a 100 ohm differential termination resistor be provided on the host board. This provides a 50 ohm single-ended termination impedance and reduces the number of external components required on the application board. See Figure 5.

NOTE

To improve electromagnetic interference (EMI), signals to the connector must be disconnected when the transceiver is removed.

In most applications using optical transceivers, additional high speed circuitry, such as clock oscillators, is present on the application board. These high speed signals often lead to noise on power supply circuits at a high spectral bandwidth which can affect the performance of transceivers. Even though the transceivers provide electro-magnetic immunity regarding emission, ingress of radiation and immunity against conductive noise must be considered.

When designing the electrical interface between the transceiver and the PHY chip, it is important to terminate the transmission line with the appropriate characteristic impedance (typically 50 ohms). It is also important to pay particular attention to pc board layout practices. Microstrip lines are recommended for optimum transmission signal quality. Termination recommendations are given for 50 ohm transmission lines. The recommended pc board layer structure is shown in Figure 8.

Vcc and GND connections should be made as short as possible. GND islands should be tied to main GND by vias or avoided if possible. Differential signal lines should be as short as possible to maintain signal integrity. Transmitter data input lines and receiver data output lines should be kept far apart to prevent crosstalk. These lines can be run orthogonally or separated with a ground plane layer. One way to maintain the separation is to place all components for the transmit circuit on one side of the board and all components for the receive circuit on the other side of the board. Vias and layer changes should be avoided. The separation between differential traces of each input or output stage can be minimized by using microstrip design rules.

L1=L2=1μH Note 1

C1=C2=C4=0.01μF-0.1μF Note 2

C3=4.7-10μF

Notes:

1 Ferrite beads could be used as an option

2 X7R or better MLC types are recommended for all capacitors

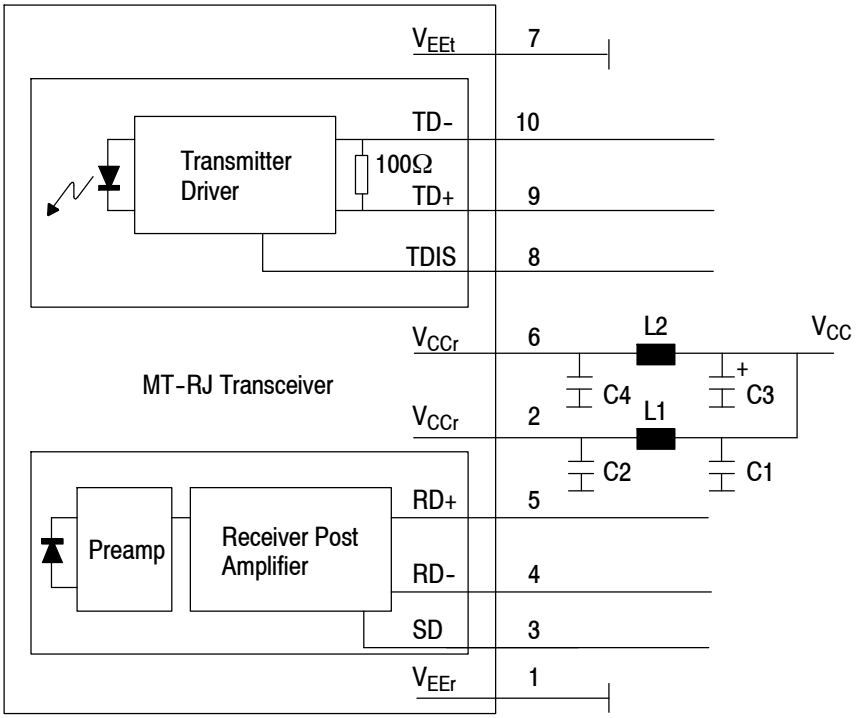


Figure 5

INTERFACING WITH GIGABIT PHY ICs

MT-RJ Gigabit Transceiver was designed to be compatible with Gigabit Ethernet integrated circuits that are commercially available today. Examples of these ICs include the Vitesse VSC7136, Applied Micro Circuits Corp (AMCC) S2046/S2047, Advanced Micro Devices (AMD) Am79761, and the Hewlett Packard HDMP-1636/1646. Each of these PHY chips include the clock and data recovery circuits, serializer/deserializer (SERDES), and the line drivers and receivers necessary to communicate using fiberoptic transceivers or copper media.

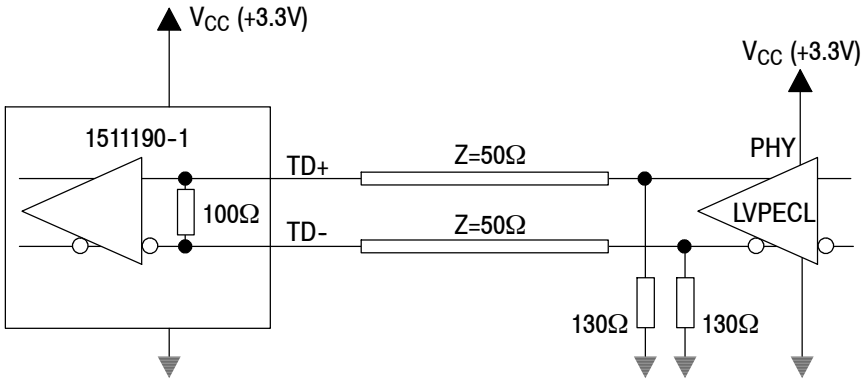
The majority of commercially available PHY chips operate from a single +3.3 V power supply but the 1511190-1 MT-RJ transceiver can operate with +5.0 V PHY chips if correctly configured. +3.3 V PHY chips use LVPECL (Low Voltage Positive Emitter Coupled Logic) compatible and +5 V PHY chips use PECL compatible interfaces for all high speed serial data I/O. Both LVPECL and PECL have a typical AC voltage swing of around 600 mV. For LVPECL, the AC signal is centered around 2 V. For PECL, the signal swings around a 3.7 V DC level. Because of this difference in DC levels, AC coupling is necessary when interfacing between LVPECL and PECL I/O.

The MT-RJ Gigabit Transceiver is provided with differential data inputs and outputs. Single-ended mode use is not recommended. Single ended operation does not take advantage of the common mode noise rejection characteristics of the differential amplifier input stages. In many cases this results in reduced signal integrity, causes excessive EMI generation, and can compromise the performance of the transceiver.

The following schematics show possible interfaces for the MT-RJ transceiver. These schematics were developed as part of the Small Form Factor (SFF) multisource agreement. Each company participating in the SFF agreement has agreed to design their transceivers to be compatible with the electrical interface recommendations contained in the following figures. Although other interface designs may provide acceptable performance, these specific configurations are recommended for true "drop-in" compatibility between the various suppliers.

Figure 6 illustrates a 3.3V transceiver to 3.3V PHY interface.

Transmitter Interface



Receiver Interface

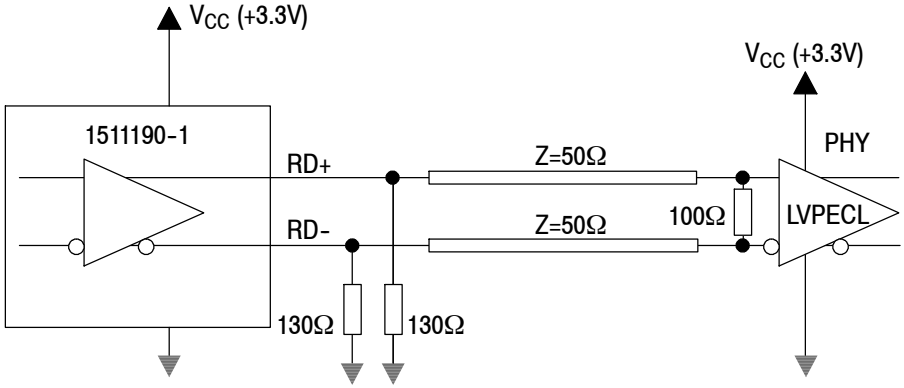
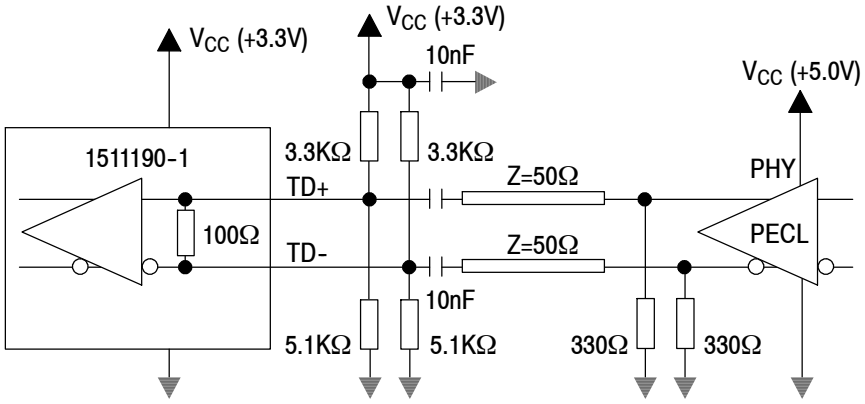


Figure 6

Figure 7 illustrates a 3.3V transceiver to 5.0V PHY interface.

Transmitter Interface



Receiver Interface

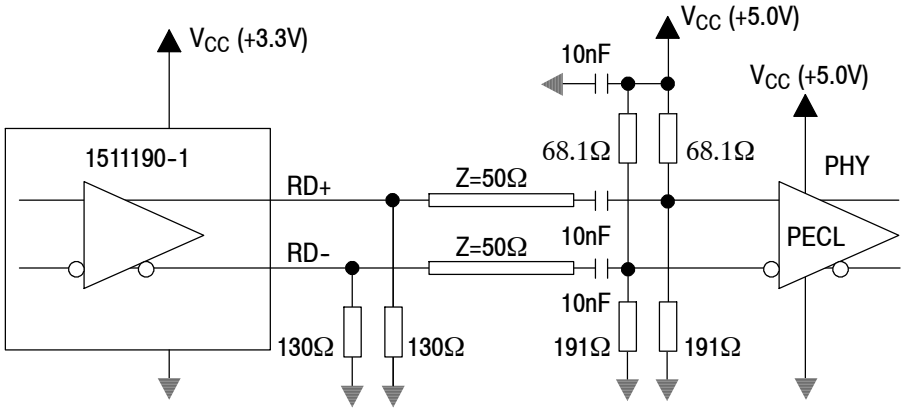


Figure 7

Figure 8 represents the recommended pc board layer structure.

Recommended PC Board Layer Structure

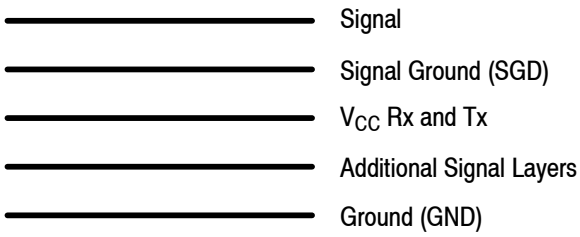


Figure 8

3.8. Transceiver Filtering

Power supplies in the system must be adequately filtered to prevent supply noise from degrading transceiver performance. The theory behind commonly used power supply filtering techniques described in text books and integrated circuit data books is covered in this document.

The recommended filter scheme separates the power supply for the transmitter and receiver. Power supply noise amplitude and frequency content is largely influenced by the type of supply used, high frequency logic and switching circuitry in the system, circuit board design, etc. For this reason, supply filter circuits should be evaluated under actual conditions before finalizing the design. Capacitors should be chosen with low effective series resistance, low dissipation factor and high Q. NPO or COG temperature characteristics are preferred because they provide more reliable performance over a wide range of environmental conditions. X7R types will also give acceptable performance; however, Y5V and Z5U should be avoided due to their large temperature and voltage coefficients. Ferrite beads used for L1 and L2 will provide higher noise attenuation because they do not possess the interwinding capacitance of a wound inductor. Refer to Figure 5.

Small surface-mount packages are recommended since they exhibit less parasitic inductance which can lower the overall effectiveness of the bypass capacitor at high frequencies. Filter capacitors should be placed close to the transceiver power and ground pins to minimize noise coupling which can occur between the filter and the transceiver.

The impedance of power supply and ground lines on the pc board must be kept low. This is necessary because the dynamic current requirements of high speed digital circuitry can interact with a non-zero impedance to cause fluctuations in the voltage delivered to the transceiver. Therefore, this impedance leads to noise on the supply lines in addition to the inherent power supply switching noise. In order to keep the impedance low, the use of dedicated power and ground planes is strongly recommended.

3.9. Cleaning the Optical Interface

Although the case of the transceiver is quite robust, care must be taken with the transceiver optics. Isopropyl alcohol is the only solvent that can be used to clean the transceiver. Filtered, dry air can be used to blow debris from the interface area. A grounded electrostatic discharge (ESD)-protected nozzle on the air hose must be used. Canned air can also be used; however, many cans contain additives in the air stream. These additives can leave a film on the optics.

Any procedures that could scratch the interface must be avoided. Any visible debris must be removed with a blast of air. It is recommended to flush the area rather than rub the lens with an alcohol-soaked swab. For stubborn or excessive dirt, the lens must be blasted with air, then flushed with alcohol, and blasted with air again.

3.10. Pin-Out Description

Figure 9 shows the MT-RJ pinout configuration. Note that there is no internal connection between the receiver and transmitter V_{CC} pins (2,6). The receiver and transmitter V_{EE} pins are internally connected to each other through internal package shielding. The two larger pins located near the optical interface provide a solid mechanical connection between the module and the circuit board. These mounting lugs should be connected to the instrument chassis ground. Note that they are electrically isolated from the signal ground plane.

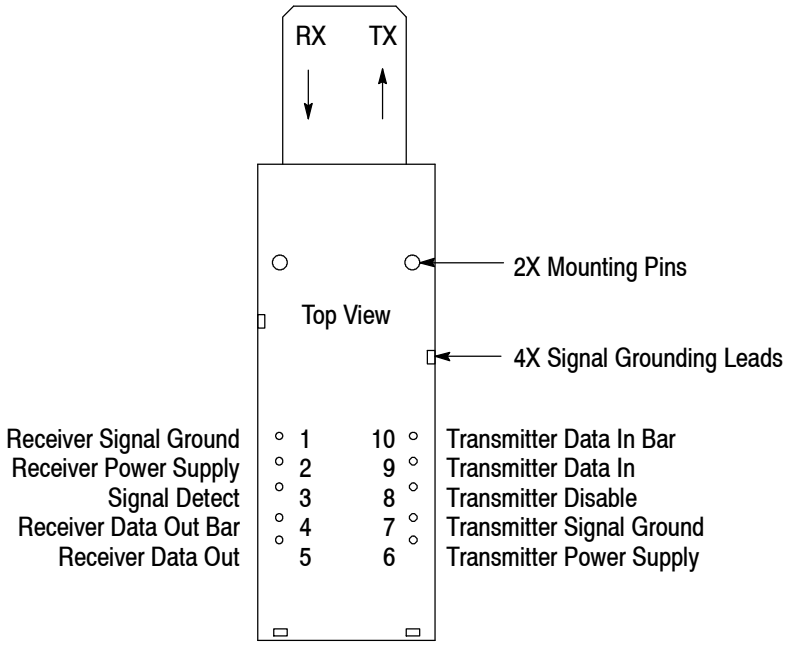


Figure 9

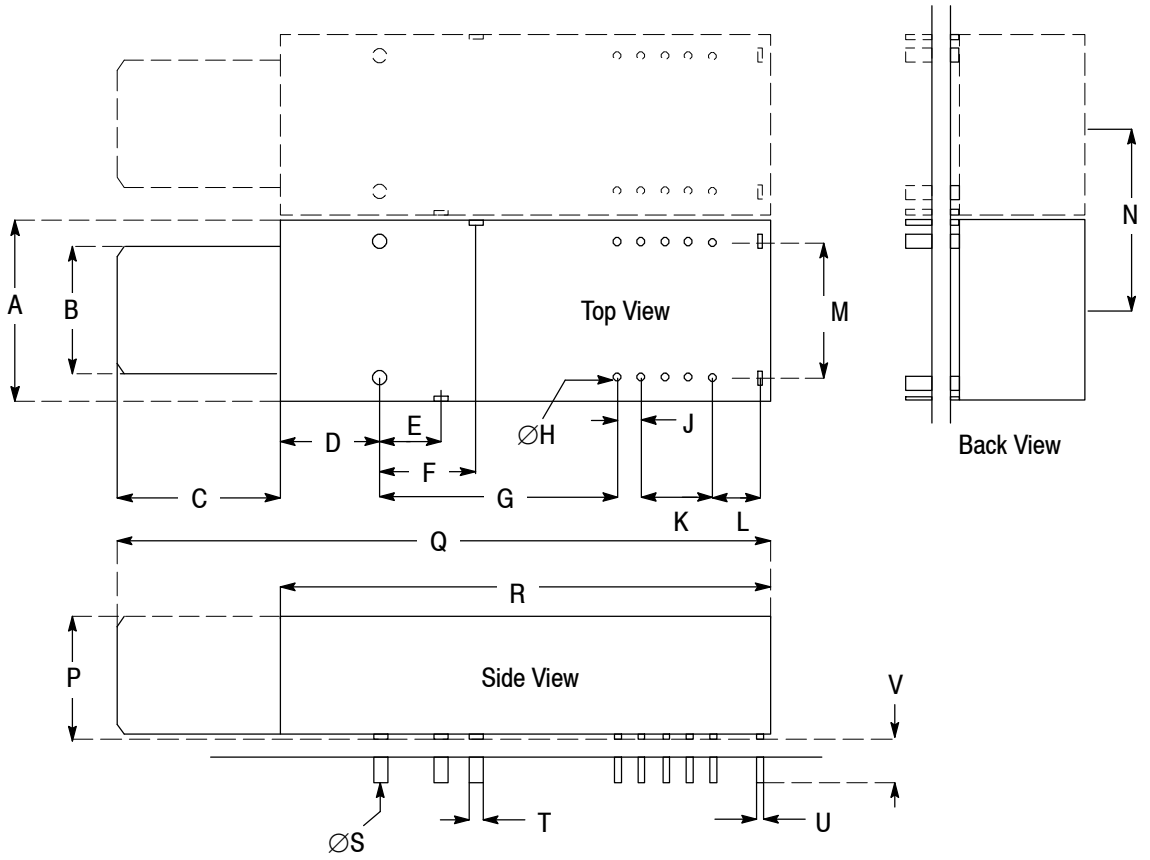
The information in Figure 10 describes the pins, lists their pin numbers, and provides a functional description of each pin.

Symbol	Pin Number	Function
Two Front Mounting Studs		Provided for mechanical attachment to the printed circuit board and ensure mechanical strength. The holes on the printed circuit board to which they attach must be connected to chassis ground.
Four Holes for Signal Grounding Leads		Connect to signal ground.
V_{EEr}	1	Receiver Signal Ground. Connect to receiver signal ground plane.
V_{CCr}	2	Receiver Power Supply.
SD	3	Signal detect. Normal Operation: Logic “1” Output. Fault Condition: Logic “0” Output.
RD-	4	Received Data Out Bar. No internal terminations are provided.
RD+	5	Received Data Out. No internal terminations are provided.
V_{CCt}	6	Transmitter Power Supply.
V_{EEt}	7	Transmitter Signal Ground.
T_{DIS}	8	Transmitter Disable Input.
TD+	9	Transmitter Data In. There is an internal 100 Ohm resistor across TD+ and TD- which provides a 50 Ohm termination for each data input.
TD-	10	Transmitter Data In Bar. There is an internal 100 ohm resistor across TD+ and TD- which provides a 50 ohm termination for each data input.

Figure 10

3.11. Installation of Transceiver - Package Outline

Figures 11,12, and 13 provide the dimensional information for installing the modules onto the pc board and through the front panel.



NOTE

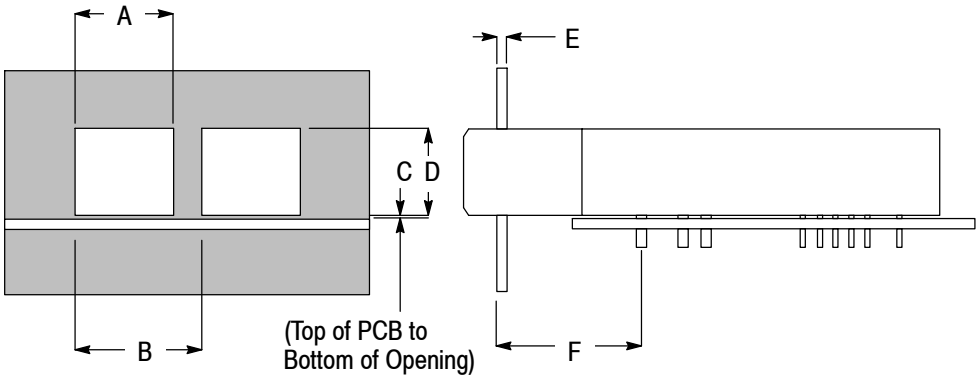
1. *Tolerance to accommodate round or rectangular leads*
2. *All 12 pins and posts are to be treated as a single pattern.*
3. *The MT-RJ optical connector has a 750-μm fiber spacing.*
4. *Refer to the MT-RJ Transceiver Pin Out Diagram for additional information.*
5. *This transceiver is supplied with an EMI gasket that fits onto the nose-piece and ensures an intimate fit between the nose-piece and the MSA defined customer front panel cut-out shown in Figure 12. Refer to Customer Drawing 1511190-1 for additional details on these gasket dimensions.*

	Millimeters			Inches				Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.		Min.	Typ.	Max.	Min.	Typ.	Max.
A	--	--	13.59	--	--	0.535	L	--	3.56	--	--	0.140	--
B	--	10.16	--	--	0.400	--	M	--	10.16	--	--	0.400	--
C	--	12.40	--	--	0.488	--	N	13.97	--	--	0.550	--	--
D	--	7.59	--	--	0.299	--	P	--	9.53	--	--	0.375	--
E	--	4.57	--	--	0.180	--	Q	--	48.89	--	--	1.925	--
F	--	7.11	--	--	0.280	--	R	--	36.42	--	--	1.434	--
G	--	17.78	--	--	0.700	--	∅S	0.97	--	1.07	0.038	--	0.042
∅H	0.41	--	.061	0.016	--	0.024	T	--	1.02	--	--	0.040	--
J	--	1.78	--	--	0.070	--	U	--	0.25	--	--	0.010	--
K	--	7.12	--	--	0.280	--	V	--	3.30	--	--	0.130	--

Figure 11

MSA Recommended MT-RJ Front Panel Opening

Figure 12 illustrates the MT-RJ panel opening.



DIMENSION	MILLIMETERS			INCHES		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	10.70	10.80	10.90	.421	.425	.429
B	13.97	---	---	.550	---	---
C	0.15	0.25	0.35	.006	.010	.014
D	9.70	9.80	9.90	.382	.386	.390
E	1.00	---	2.50	.039	---	.984
F	15.50	---	16.25	.610	---	.640

Figure 12

MSA Recommended Circuit Board Layout

Figure 13 describes the MSA recommended circuit board layout for the MT-RJ Transceiver placed at 13.97 [.550] spacing.

MSA Recommended Circuit Board Layout

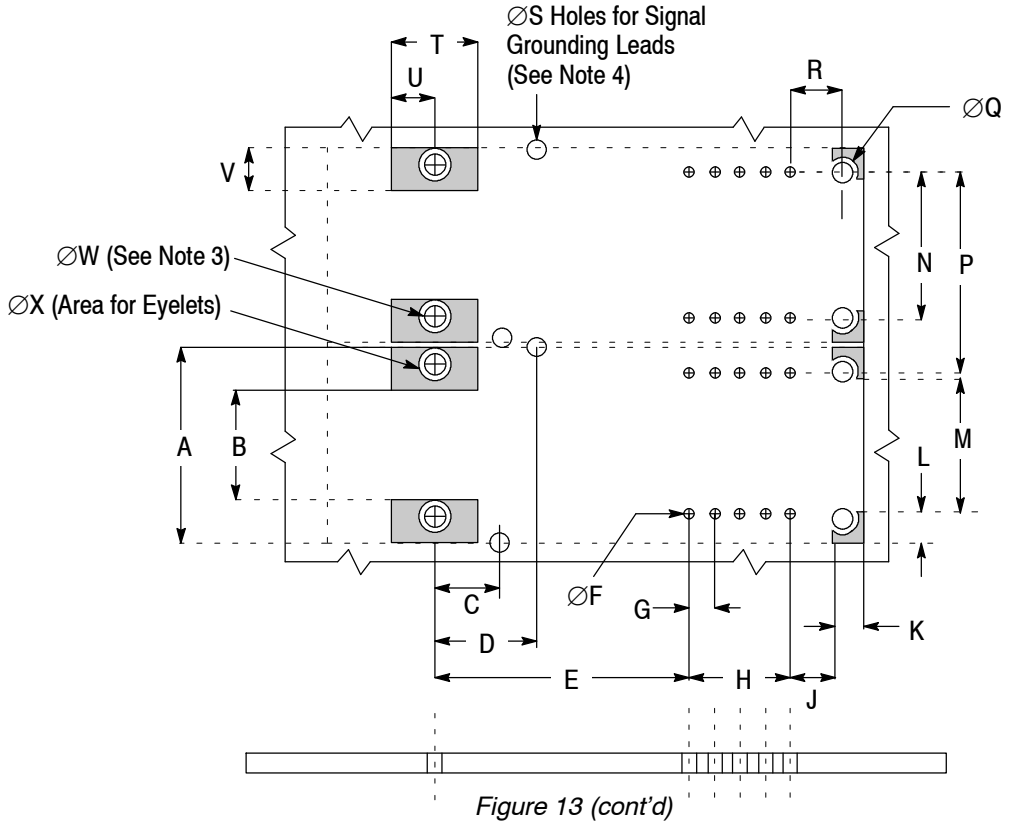


Figure 13 (cont'd)

NOTE

1. The shaded areas are keep-out areas reserved for housing standoffs. No metal traces or ground connection in keep-out areas.
2. The 10-pin module implementation requires only 16 pcb holes.
3. Solder posts should be soldered to the printed circuit board for mechanical strength and these pcb holes should be connected to chassis ground.
4. These four holes for signal grounding leads must be connected to signal ground on the printed circuit board.

DIM.	MILLIMETERS			INCHES			DIM.	MILLIMETERS			INCHES		
	Min.	Typ.	Max.	Min.	Typ.	Max.		Min.	Typ.	Max.	Min.	Typ.	Max.
A	---	13.34	---	---	.525	---	M	---	9.59	---	---	.378	---
B	---	7.59	---	---	.299	---	N	---	10.16	---	---	.400	---
C	---	4.57	---	---	.180	---	P	13.97	---	---	.550	---	---
D	---	7.11	---	---	.280	---	∅Q	---	---	2.29	---	---	.090
E	---	17.78	---	---	.700	---	R	---	3.56	---	---	.140	---
∅F	0.71	---	0.91	.028	---	.036	∅S	1.30	---	1.50	.051	---	.059
G	---	1.78	---	---	.070	---	T	---	6.00	---	---	.236	---
H	---	7.12	---	---	.280	---	U	---	3.00	---	---	.118	---
J	---	3.08	---	---	.121	---	V	---	3.00	---	---	.118	---
K	---	2.00	---	---	.079	---	∅W	1.30	---	1.50	.051	---	.059
L	---	2.00	---	---	.079	---	∅X	---	---	2.29	---	---	.090

Figure 13 (end)

3.12. Reliability

Fiber optic transceivers are considered high-reliability parts. Reliability applies not only to catastrophic failure of the part but also to its ability to transmit data reliably. There should be no bad data because of transceiver failure.

Fiber optic transceivers, like other semiconductor devices, follow the typical bathtub curve of reliability. For a typical batch of components, some parts will fail early—within the first few weeks or months of operation. This infant mortality stems from the inability of the parts to withstand the stresses of operation. After these parts have failed early in the life cycle, the remaining components will exhibit reliable, stable operation over many years. Eventually, after many years, some other parts will fail.

Early life failures can be caught during manufacturing and eliminated from shipped products by stressing component parts during manufacture and by burning in completed transceivers. The burn-in procedure involves temperature cycling the transceivers between the two extremes of -40°C and +85°C [-40°F and +185°F] for 13 cycles, with a 30-minute dwell at each extreme. All component-level reliability procedures are based on Bellcore TA-NWT-000983.

The end of life (EOL) for an optical transceiver occurs when its operation degrades a defined amount. The amount of acceptable degradation before EOL depends on the application: 3.0 dB for telecommunication applications and 1.5 dB for data communication applications.

CAUTION

If components are damaged, they must be removed and replaced.

4. QUALIFICATION

A complete list of current qualifications cannot be maintained on this document; however, the following reference qualifications are representative of these transceivers. Qualification for specific transceiver part numbers can be obtained by contacting PRODUCT INFO at the number at the bottom of page 1.

Center for Devices and Radiological Health (CDRH) under Accession 9122051-07 and 9122051-08
Technischen Überwachungs-Vereine (TUV) Certificate B 02 05 46940 001
Underwriters Laboratories Inc. (UL) under File E141081

5. TOOLING

No tooling is required for installing the transceiver.

6. VISUAL AID

Figure 14 shows a typical application of Gigabit Ethernet Multimode SFF MT–RJ Transceivers. This illustration should be used by production personnel to ensure a correctly applied product. Applications which DO NOT appear correct should be inspected using the information in the preceding pages of this specification and in the instructional material shipped with the product or tooling.

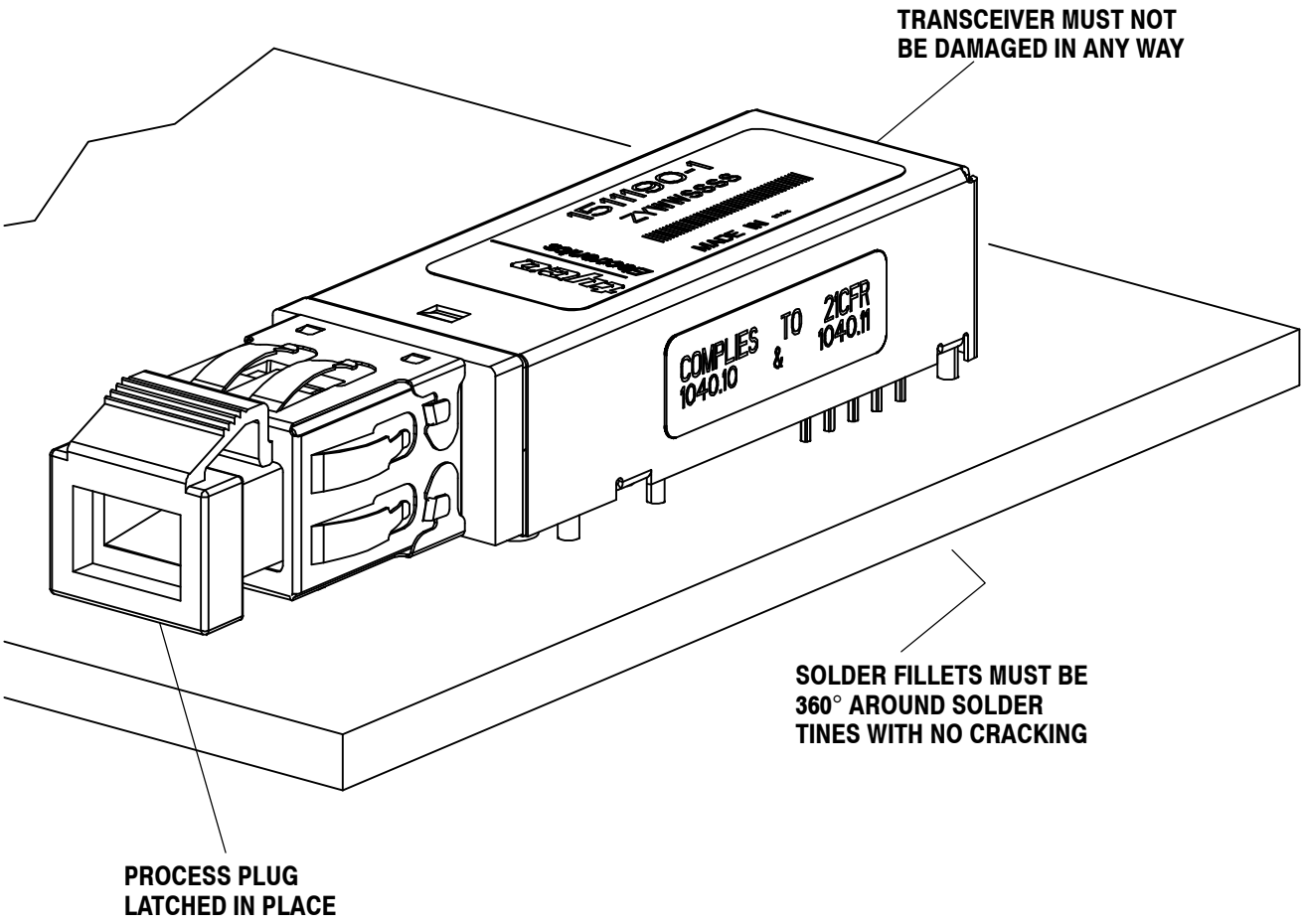


FIGURE 14. VISUAL AID